Energy Engineering

Tech Science Press

Doi:10.32604/ee.2025.074465

ARTICLE

An Improved Inverted SVPWM for Common-Mode Voltage Suppression and High-Order Harmonics Dispersion in PMSMs

Meng Zhang[1], Lijuan Zhang[2], Jie Zhang[1], Shiliang Miao[2], Jiangong Yang[2], Yajun Zhao[1,*] and Feifei Bu[1]

[1]Department of Electrical Engineering and the Center for More-Electric-Aircraft Power System, Nanjing University of Aeronautics and Astronautics, Nanjing, 211106, China

[2]Beijing Research Institute of Precise Mechanics and Controls, Beijing, 100076, China

*Corresponding Author: Yajun Zhao. Email: zhaoyajun@nuaa.edu.cn

Received: 11 October 2025; Accepted: 11 December 2025; Published: 18 June 2026

ABSTRACT: Conventional electric servo drive systems suffer from high common-mode voltage (CMV) due to the use of zero vectors in Space Vector Pulse Width Modulation (SVPWM). To mitigate this issue, this paper proposes an inverted SVPWM (I-SVPWM) strategy. By simply inverting the switching actions of a specific phase, this strategy avoids the use of zero vectors and achieves an effect similar to Active Zero-State PWM (AZSPWM), thereby effectively suppressing common-mode voltage. Compared with AZSPWM, the proposed method eliminates the need to recalculate vector action times or design new switching sequences. It can be seamlessly implemented by applying a straightforward inversion logic to the switching signals of one phase based on conventional SVPWM, which significantly enhances its practical convenience. Furthermore, similar to AZSPWM, the elimination of zero vectors in I-SVPWM leads to an increase in harmonic peaks in the output voltage and current compared to conventional SVPWM. To address this, an Alternating Inverted SVPWM (AI-SVPWM) strategy is introduced. Since the sequence of vector actions differs in each cycle, the high and low levels of the line voltage shift locally within each switching period. This causes the reconstruction of harmonic and even fundamental components in the output waveform, thereby reducing harmonic peaks at even multiples of the switching frequency. Simulations of SVPWM, AZSPWM1, AZSPWM3, I-SVPWM, and AI-SVPWM are conducted in MATLAB/Simulink. The results confirm that the proposed strategies effectively reduce common-mode voltage. Although AI-SVPWM achieves a lower harmonic amplitude compared to I-SVPWM, conventional SVPWM still maintains superior steady-state performance.

KEYWORDS: PMSM; SVPWM; common-mode voltage; harmonic dispersion; switching sequences

1 Introduction

Permanent magnet synchronous motors (PMSMs) have been increasingly adopted across the field of new energy due to their high power density, superior efficiency, and excellent dynamic response. They now serve as the prime mover in a wide range of applications, including drive systems for new energy vehicles, pump lift motors in photovoltaic water pump systems, motor drives for energy storage systems, and wind power generators [1–3]. Currently, electric servo drive systems primarily utilize PWM strategies to control the inverter's switching states, thereby outputting voltage pulse trains. The desired voltage waveform is equivalently obtained by controlling the pulse width and sequence period to power the servo motor. Reference [4] directly compares various PWM techniques for PMSM drives and analyzes current quality (THD) and inverter efficiency. Although Sinusoidal PWM (SPWM) is simple to implement, it suffers from

high current harmonic content and low DC bus voltage utilization. Space Vector Pulse Width Modulation (SVPWM), on the other hand, approximates the rotational trajectory of the ideal flux linkage using voltage vectors corresponding to different inverter switching states. Compared to SPWM, SVPWM improves DC bus voltage utilization. Traditional SVPWM strategies generate significant high-frequency harmonics at the switching frequency and its multiples, which constitute a major source of conducted Electromagnetic Interference (EMI) in servo drive systems. Furthermore, the common-mode voltage produced by high-frequency PWM can induce shaft voltage and current in the motor, leading to bearing corrosion and reduced motor lifespan [5–7]. Electromagnetic Compatibility (EMC) standards in the field of new energy are now more critical than ever. The suppression of PMSM harmonics and common-mode voltage has thus transitioned from an optional improvement to a mission-critical requirement for achieving high performance and reliability—especially with the application of wide-bandgap semiconductor devices (such as SiC and GaN), whose higher switching frequencies and faster switching speeds have made EMC issues in PMSM systems more pronounced [8]. This capability is pivotal to the core competitiveness of new energy products and is a fundamental enabler for the continued advancement of the electric vehicle, wind power, and solar power industries [9]. Active suppression of conducted EMI in servo drive systems can be achieved through modifications to conventional PWM strategies, an approach that is equally applicable to grid-connected photovoltaic inverters [10].

One approach involves modifying the inverter's circuit structure or adding hardware components, such as common-mode filters and common-mode chokes, or altering the topology. However, these strategies increase the cost and complexity of the drive system and exhibit poor universality [11–14].

Another approach focuses on the optimization of PWM pulse patterns. Since the amplitude of the inverter output common-mode voltage is related to different switching state combinations, switching state combinations that yield smaller common-mode voltage can be used to equivalently replace those that produce larger common-mode voltage. When all three-phase bridge arms are switched to the upper or lower arms, meaning the inverter outputs a zero voltage vector, the output common-mode voltage is at its maximum. Consequently, researchers have proposed zero-vector elimination common-mode voltage suppression strategies, which primarily include strategies such as remote state PWM (RSPWM), near state PWM (NSPWM), and Active Zero State PWM (AZSPWM) [15]. The implementation principles are illustrated in Fig. 1, where AZSPWM can be further divided into AZSPWM1 and AZSPWM3 based on the different switching state combinations employed [16–18].

In RSPWM (Fig. 1a), the reference vector is synthesized exclusively using three non-adjacent and non-zero voltage vectors, which fundamentally excludes the use of zero vectors. However, this method fails to synthesize the desired reference vector when the modulation index is high.

In contrast, NSPWM (Fig. 1b) constructs its synthesis path using only three adjacent non-zero vectors. A key limitation of this strategy is its inability to accurately synthesize the required reference vector at low modulation indices.

The switching sequences for AZPWM1 and AZPWM3 (Fig. 1c,d) demonstrate the core 'active zero-state' concept [19]. This is achieved by inserting a pair of non-zero vectors with equal duration but opposite directions (such as U_k and U_{k+3}) to replace the conventional zero-vector intervals. The distinction lies in the vector selection: in AZPWM3, the opposing vector pair includes one vector that is also an active vector used for synthesizing the reference vector, effectively meaning only three non-zero vectors are utilized per cycle [20–22].

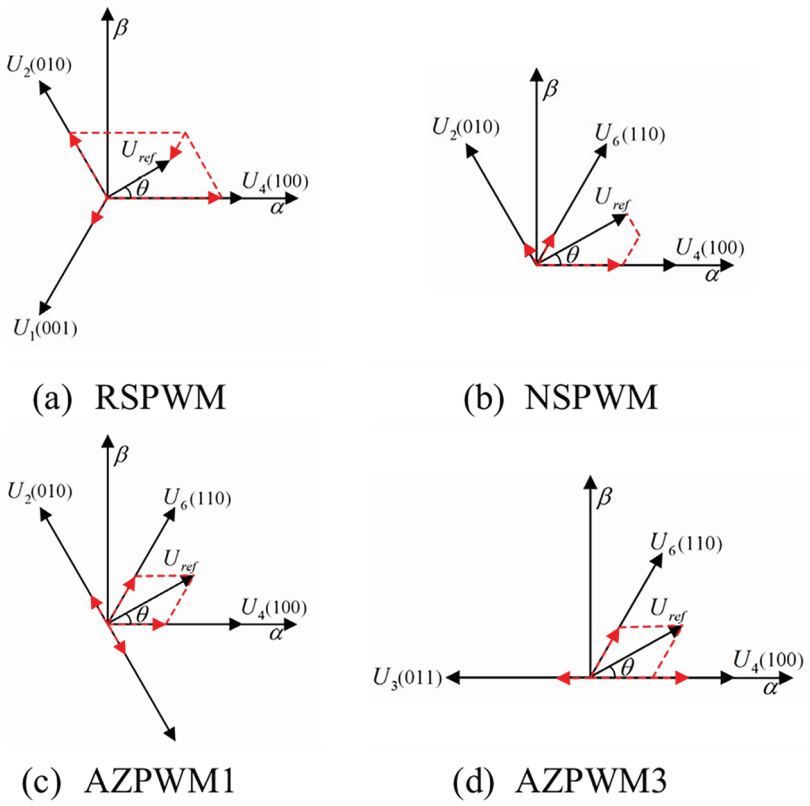


Figure 1: Four types of zero-vector-free common-mode voltage suppression strategies

The distinctions among these methods lie primarily in the switching state combinations used to replace the zero vectors, and all can achieve effective common-mode voltage suppression. However, these strategies invariably impact the system's control performance to some extent and require the redesign of the SVPWM control algorithm.

In [23], focusing on harmonic optimization for three-level inverters, a Variable Zero Vector Position Modulation strategy is proposed. By adjusting the peak position of the zero-vector in SVPWM (such as through sawtooth carrier offset), harmonic distribution is controlled while data is embedded into the switching ripple. In [24], targeting interleaved parallel inverter systems, a combined harmonic optimization strategy of "improved SVPWM + sequence interleaving" is proposed. Low common-mode voltage modulation strategies, namely AZPWM and NSPWM, are selected as the base modulation schemes. First, the analytical expressions of the DC bus current for three PWM strategies (SVPWM, AZPWM, NSPWM) are derived through time-domain modeling. Then, an offline numerical optimization algorithm is used to find the optimal interleaving offset synchronized with the PWM sequence, enabling the DC bus harmonics of the two inverters to cancel each other out. In [25], addressing the issue of PWM frequency harmonics in three-level inverters, a Zero-sequence Switching SVPWM strategy is proposed. Based on the traditional single-edge SVPWM, this strategy exchanges the zero-vector sequence in adjacent carrier cycles, thereby doubling the equivalent carrier frequency and eliminating odd-order switching frequency harmonics. In [26], the four possible placement sequences of zero vectors in SVPWM are analyzed and discussed, and four rotation methods are evaluated under identical conditions, thus providing new insights for harmonic optimization of SVPWM modulation strategies. In [27], addressing harmonic optimization for six-phase inverters, the core innovation lies in proposing a novel SVPWM switching sequence. By optimally selecting switching

states with "minimum/zero common-mode voltage" and ensuring balanced distribution of switching vectors in the subspace, voltage and current components are nullified, thereby suppressing harmonic generation at the source. In [28], the core innovation for a five-level NPC transformerless PV grid-tied inverter is a CMV suppression strategy that connects the DC-link terminals to a common grid-neutral point via parasitic capacitors, eliminating the CM current loop potential difference, while switching state control maintains DC-link capacitor balance and confines the CMV within a stable range without high-frequency spikes.

Based on the foundation of prior research concerning low common-mode voltage, the aforementioned studies achieve harmonic suppression by optimizing switching sequences for different inverter topologies. In fact, common-mode voltage can be effectively suppressed simply by inverting the switching actions of one phase. Specifically, within one switching cycle, while maintaining the total turn-on duration of that phase unchanged, its turn-on time can be symmetrically distributed on both sides with respect to the center of the cycle. Compared to the aforementioned zero-vector elimination strategies, this strategy, referred to as inverted SVPWM (I-SVPWM), eliminates the need to recalculate vector action times or design new switching sequences, thereby offering significantly greater implementation convenience in practice. Furthermore, by alternately inverting different phases over time, the sequence of vector actions varies in each cycle, effectively implementing multiple rotation modes to further optimize harmonic performance.

The core contributions of this work are twofold:

1. The theory behind I-SVPWM for common-mode voltage suppression is proposed and analyzed.
2. An alternating inverted SVPWM (AI-SVPWM) strategy is further proposed to optimize the harmonic spectrum amplitude, with the mechanism for high-order harmonics dispersion derived.

The remainder of this paper is organized as follows: Section 2 details the theoretical foundation of SVPWM and the principle of the proposed I-SVPWM for common-mode voltage reduction. Section 3 presents the AI-SVPWM and the principle of its harmonic optimization implementation. Section 4 presents and discusses simulation results regarding current THD, torque ripple, common-mode voltage, and harmonic spectra. Finally, Section 5 concludes the paper.

2 Operating Principle of Inverted SVPWM (I-SVPWM) for Common-Mode Voltage Suppression

The structure of a three-phase inverter bridge for a PMSM drive is shown in Fig. 2. To prevent shoot-through in a bridge leg, the high-side and low-side switches are operated complementarily. Defining the high-side switch being ON as '1' and the low-side switch being ON as '0', the three-phase inverter bridge has eight possible switching states, as shown in Fig. 3: 000, 001, 010, 011, 100, 101, 110, 111. These eight switching states correspond to eight basic space voltage vectors. Among them, the states 000 and 111 do not produce an effective output voltage; thus, their corresponding space voltage vectors are zero vectors, while the others are active vectors.

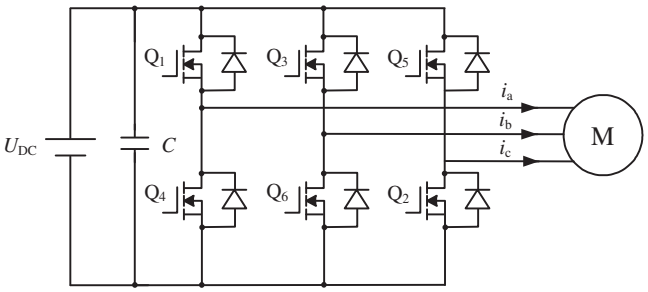


Figure 2: Structure of a three-phase inverter bridge for a PMSM drive

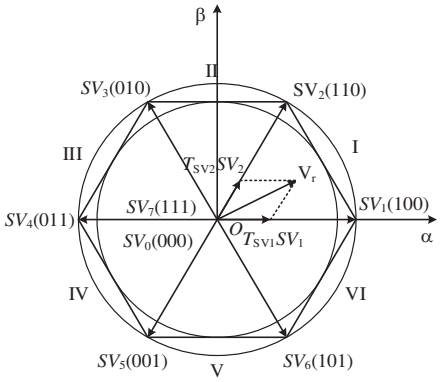


Figure 3: Basic space voltage vectors

Since the inverter can only output a finite set of eight vectors with fixed magnitudes, the continuously rotating reference space vector $\mathbf{V}_r$ must be synthesized from these basic vectors according to the volt-second balance principle. As shown in Fig. 3, assuming the rotating vector $\mathbf{V}_r$ is located in Sector I and acts for a duration T_s (T_s is the sampling period), it can be synthesized from $S\mathbf{V}_1$, $S\mathbf{V}_2$, and the zero vectors. The synthesis equation satisfying the volt-second balance principle is:

$$T_s\mathbf{V}_r = T_s\mathbf{V}_r e^{j\theta} = \mathbf{V}_r\left(\cos\theta + j\sin\theta\right) = T_{sv1}S\mathbf{V}_1 + T_{sv2}S\mathbf{V}_2 + T_{sv0}S\mathbf{V}_0 + T_{sv7}S\mathbf{V}_7 \tag{1}$$

Although the zero vectors do not contribute to the output voltage, they fill the remaining time not occupied by the active vectors. Solving the equation yields the dwell times for each vector:

$$T_{sv1} = \frac{V_r \sin\left(\frac{\pi}{3} - \theta\right)}{V_m \sin\frac{\pi}{3}} \times T_s, \quad T_{sv2} = \frac{V_r \sin\theta}{V_m \sin\frac{\pi}{3}} \times T_s \tag{2}$$

$$T_{sv0/7} = \left(T_s - T_{sv1} - T_{sv2}\right)/2 \tag{3}$$

Fig. 4 illustrates the typical switching sequence of active and zero vectors for different sectors in standard SVPWM. If the zero-vector time is equally shared between $V0$ and $V7$, it constitutes the standard or conventional space vector modulation.

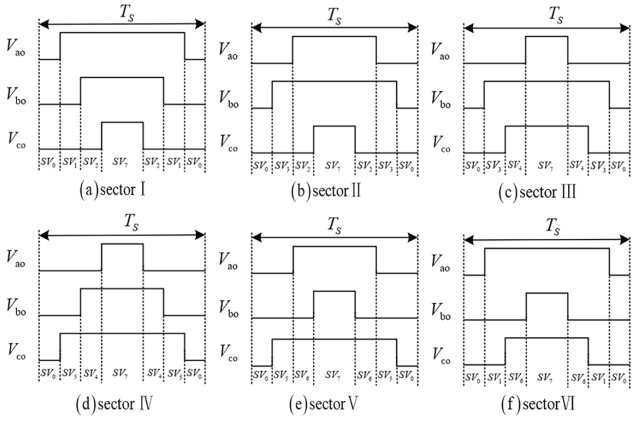


Figure 4: Switching sequences for Sectors I~VI

The potential difference U_{Ng} between the neutral point N of the three-phase windings and the reference ground g is defined as the common-mode voltage V_{CM}. For a three-phase inverter, the common-mode voltage can be expressed as:

$$V_{CM} = U_{Ng} = \frac{U_{AO} + U_{BO} + U_{CO}}{3} \tag{4}$$

When all three bridge arms are switched to either the upper or lower switches, meaning the inverter outputs a zero voltage vector, the output common-mode voltage reaches its maximum, resulting in a common-mode voltage with a peak value of $U_{dc}/2$. Therefore, researchers have proposed zero-vector elimination strategies, which use other switching state combinations to replace the zero vectors, thereby reducing the common-mode voltage amplitude to within $U_{dc}/6$.

In fact, the common-mode voltage can be suppressed simply by inverting the switching action of the B-phase. Specifically, within one switching cycle, the switching-on time T_{bk} of the B-phase is distributed symmetrically from the center to both sides while maintaining the total B-phase switching-on duration unchanged, as illustrated for Sector I in Fig. 5. This does not affect the equivalence of the output voltage. In practical implementation, the "inversion" can be achieved by either complementing the switching instants of phase B relative to the original sequence and subsequently swapping the drive signals for the upper and lower switches of phase B, or alternatively by exchanging the counting modes between the upper and lower bridge arms.

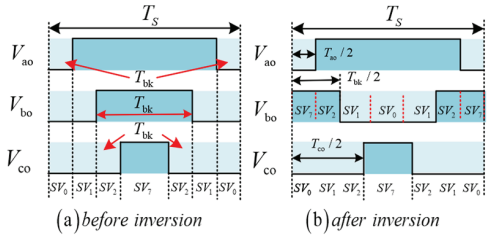


Figure 5: Switching sequences of traditional SVPWM and Inverted SVPWM (Sector I)

For the standard SVPWM ($T_{sv0} = T_{sv7}$) with phase B signal inversion, the switching sequences for all six sectors are shown in Fig. 6. Within one cycle, the turn-off time for phase A switches T_{ao}, the turn-on time for phase B switches T_{bk}, and the turn-off time for phase C switches T_{co} are specifically defined as follows across different sectors:

$$\begin{cases} T_{ao} = T_{sv0} \\ T_{bk} = T_{sv2} + T_{sv7} \\ T_{co} = T_{sv0} + T_{sv1} + T_{sv2} \end{cases} \quad \text{with } \frac{T_{ao}}{2} < \frac{T_{bk}}{2} < \frac{T_{co}}{2} \quad \text{sectorI} \tag{5}$$

$$\begin{cases} T_{ao} = T_{sv0} + T_{sv3} \\ T_{bk} = T_{sv2} + T_{sv3} + T_{sv7} \\ T_{co} = T_{sv0} + T_{sv2} + T_{sv3} \end{cases} \quad \text{with } \frac{T_{ao}}{2} < \frac{T_{bk}}{2} = \frac{T_{co}}{2} \quad \text{sector II} \tag{6}$$

$$\begin{cases} T_{ao} = T_{sv0} + T_{sv3} + T_{sv4} \\ T_{bk} = T_{sv3} + T_{sv4} + T_{sv7} \\ T_{co} = T_{sv0} + T_{sv3} \end{cases} \quad \text{with } \frac{T_{ao}}{2} = \frac{T_{bk}}{2} > \frac{T_{co}}{2} \quad \text{sector III} \tag{7}$$

$$\begin{cases} T_{ao} = T_{sv0} + T_{sv4} + T_{sv5} \\ T_{bk} = T_{sv4} + T_{sv7} \\ T_{co} = T_{sv0} \end{cases} \text{with } \frac{T_{ao}}{2} > \frac{T_{bk}}{2} > \frac{T_{co}}{2} \quad \text{sector IV} \tag{8}$$

$$\begin{cases} T_{ao} = T_{sv0} + T_{sv5} \\ T_{bk} = T_{sv7} \\ T_{co} = T_{sv0} \end{cases} \text{with } \frac{T_{ao}}{2} > \frac{T_{bk}}{2} = \frac{T_{co}}{2} \text{ sectorV} \tag{9}$$

$$\begin{cases} T_{ao} = T_{sv0} \\ T_{bk} = T_{sv7} \\ T_{co} = T_{sv0} + T_{sv1} \end{cases} \text{with } \frac{T_{ao}}{2} = \frac{T_{bk}}{2} < \frac{T_{co}}{2} \quad \text{sector VI} \tag{10}$$

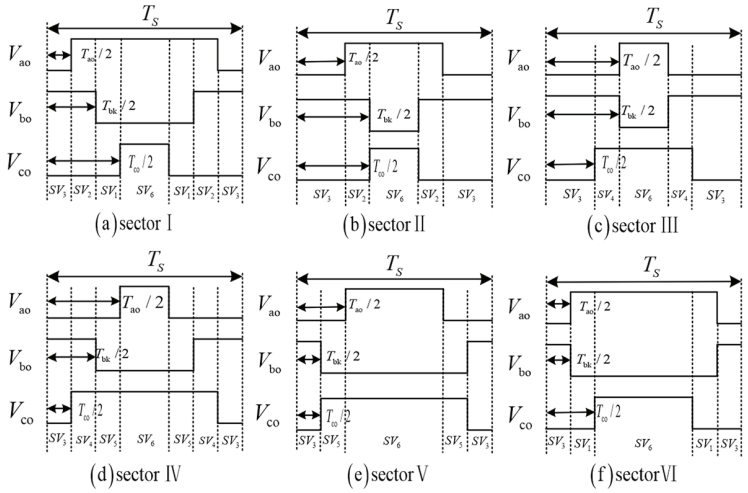


Figure 6: Switching sequences of traditional SVPWM and Inverted SVPWM (I-SVPWM)

It can be observed that after inverting the B-phase, the following equation always holds, thereby avoiding the use of zero vectors.

$$\min\left(\frac{T_{a0}}{2}, \frac{T_{co}}{2}\right) \le \frac{T_{bk}}{2} \le \max\left(\frac{T_{a0}}{2}, \frac{T_{co}}{2}\right) \tag{11}$$

The implementation of the SVPWM algorithm mainly involves three key steps: the sector determination of the reference voltage vector, the calculation of the action times of non-zero vectors and zero vectors in each sector, and the determination of vector switching points in each sector. Finally, by comparing a triangular carrier signal of a specific frequency with the vector switching points of each sector, the PWM pulse signals required by the converter can be generated. For the SVPWM with inverted B-phase switching action, we only need to make the three-phase voltage switching time points satisfy Eq. (12), and then swap the drive signals of the upper and lower bridge arms of Phase B.

$$\begin{cases} T'_{\text{cm1}} = T_{\text{cm1}} \\ T'_{\text{cm2}} = T_s/2 - T_{\text{cm2}} \\ T'_{\text{cm3}} = T_{\text{cm3}} \end{cases} \tag{12}$$

here, T_{cm1}, T_{cm2} and T_{cm3} are respectively the switching time points for the three-phase voltages of SVPWM.

Compared with AZSPWM1 and AZSPWM3, the specific vector action sequences of the three methods in each sector are contrasted in Table 1. The principle also involves replacing the zero vector's action time with

a pair of non-zero vectors that are opposite in direction and equal in duration. The advantage of this method is that it does not require recalculating the action time of each vector or designing new switching sequences. Instead, it seamlessly achieves the goal by flipping the switching action of a specific phase in traditional SVPWM. By applying simple inversion logic to the switching signal of one phase, the practical convenience is greatly enhanced, and the output current THD will be reduced, which will be verified in the simulation in Section 4. Moreover, AZSPWM1 and AZSPWM3 can be implemented by flipping the switching action of the corresponding phase in different sectors. However, similar to AZSPWM, due to the elimination of zero vectors, the total harmonic distortion (THD) of the output voltage in Inverted SVPWM is slightly higher than that in traditional SVPWM. Therefore, while suppressing the common-mode voltage of the inverter, improving the waveform quality of the output voltage and current remains an important research direction for zero vector elimination PWM strategies.

Table 1: Action sequence of non-zero vectors for different common-mode voltage suppression strategies

Sector	AZSPWM1	AZSPWM3	I-SVPWM
I	$V_3 \rightarrow V_2 \rightarrow V_1 \rightarrow V_6 \rightarrow V_1 \rightarrow V_2 \rightarrow V_3$	$V_2 \rightarrow V_1 \rightarrow V_5 \rightarrow V_1 \rightarrow V_2$	$V_3 \rightarrow V_2 \rightarrow V_1 \rightarrow V_6 \rightarrow V_1 \rightarrow V_2 \rightarrow V_3$
II	$V_4 \rightarrow V_3 \rightarrow V_2 \rightarrow V_1 \rightarrow V_2 \rightarrow V_3 \rightarrow V_4$	$V_3 \rightarrow V_2 \rightarrow V_6 \rightarrow V_2 \rightarrow V_3$	$V_3 \rightarrow V_2 \rightarrow V_6 \rightarrow V_2 \rightarrow V_3$
III	$V_5 \rightarrow V_4 \rightarrow V_3 \rightarrow V_2 \rightarrow V_3 \rightarrow V_4 \rightarrow V_5$	$V_4 \rightarrow V_3 \rightarrow V_1 \rightarrow V_3 \rightarrow V_4$	$V_3 \rightarrow V_4 \rightarrow V_6 \rightarrow V_4 \rightarrow V_3$
IV	$V_6 \rightarrow V_5 \rightarrow V_4 \rightarrow V_3 \rightarrow V_4 \rightarrow V_5 \rightarrow V_6$	$V_5 \rightarrow V_4 \rightarrow V_2 \rightarrow V_4 \rightarrow V_5$	$V_3 \rightarrow V_4 \rightarrow V_5 \rightarrow V_6 \rightarrow V_5 \rightarrow V_4 \rightarrow V_3$
V	$V_1 \rightarrow V_6 \rightarrow V_5 \rightarrow V_4 \rightarrow V_5 \rightarrow V_6 \rightarrow V_1$	$V_6 \rightarrow V_5 \rightarrow V_3 \rightarrow V_5 \rightarrow V_6$	$V_3 \rightarrow V_5 \rightarrow V_6 \rightarrow V_5 \rightarrow V_3$
VI	$V_2 \rightarrow V_1 \rightarrow V_6 \rightarrow V_5 \rightarrow V_6 \rightarrow V_1 \rightarrow V_2$	$V_1 \rightarrow V_6 \rightarrow V_4 \rightarrow V_6 \rightarrow V_1$	$V_3 \rightarrow V_1 \rightarrow V_6 \rightarrow V_1 \rightarrow V_3$

3 Improved I-SVPWM Considering Harmonic Amplitude Suppression

Going a step further, as shown in Fig. 7, we can alternately invert phases A, B and C over time (AI-SVPWM), rather than inverting only the B-phase. Both switching modes—inverting only the B-phase and alternately inverting A, B, C phases—do not alter the macroscopic sector sequence, and the dwell times of the vectors in each switching cycle are identical; thus, their fundamental effect is equivalent. However, because the sequence of vector actions differs in each cycle, the high and low levels of the line voltage within each switching cycle shift locally. This leads to a restructuring of the harmonic components and even the fundamental component in the output waveform, causing some to increase while others decrease.

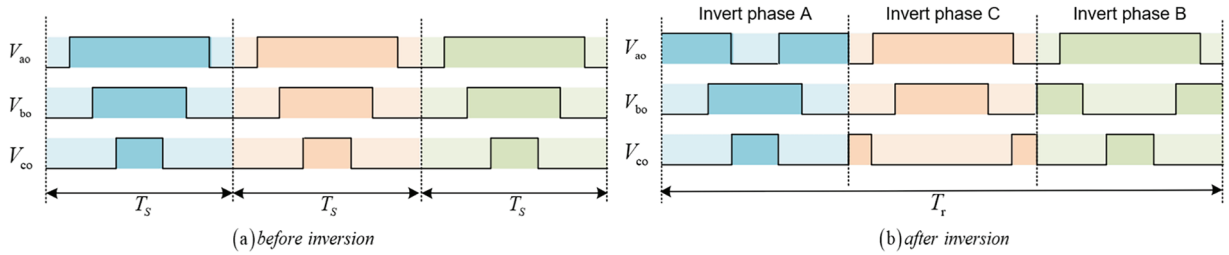


Figure 7: Alternately invert phases A, B, and C

Traditional SVPWM is designated Mode A, and its line voltage $V_{AB}(t)$ waveform function is denoted as $V_{AB\_A}(t)$.

I-SVPWM with the B-phase inverted is Mode B. Its waveform $V_{AB\_B}(t)$ can be expressed as:

$$V_{AB\_B}(t) = V_{AB\_A}(t) + P_B(t) \tag{13}$$

where $P_B(t)$ is a disturbance pulse function representing the extra voltage pulses introduced by replacing the zero vectors.$P_B(t)$, within each switching cycle T_s, consists of a symmetric pulse pair with a duration of $T_{sv0/7}$ (half of the total zero-vector time) and an amplitude of V_{DC}. Its period is the switching period T_s.

According to Fourier analysis, the spectrum of such a periodic pulse train $P_B(t)$ is a discrete line spectrum, with its energy concentrated around integer multiples of the switching frequency f_s, i.e., nf_s. Its amplitude can be calculated using the Sinc function:

$$C_n = \frac{2}{T_s} \int_{-T_s/2}^{T_s/2} P_B(t)\, e^{-jn\omega_s t} dt \tag{14}$$

For a symmetric square wave pulse, the harmonic amplitude at nf_s is proportional to $\frac{\sin(\pi n f_s \tau)}{\pi n f_s \tau}$, where τ is the duty cycle ($T_{sv0/7}$).

Mode B superimposes a discrete harmonic spectrum $\mathcal{F}\{P_B(t)\}$, potentially with significant amplitude, onto the original spectrum of $V_{AB\_A}(t)$. These harmonics are centered at nf_s. This leads to an increase in voltage and current THD and may cause pronounced electromagnetic noise.

AI-SVPWM is Mode C. Here, the disturbance function $P_C(t)$ is no longer a simple periodic function with period T_s. Its amplitude and polarity vary at a lower frequency—specifically, the three-phase inversion rotation frequency f_r.

We can model $P_C(t)$ as:

$$P_C(t) = m(t) \cdot P_B(t) \tag{15}$$

where: $P_B(t)$ is the fixed, period-T_s disturbance pulse from Mode B. $m(t)$ is a modulation function that reflects the modulation of the disturbance pulse's polarity and effectiveness by different sectors. The period of $m(t)$ is the three-phase inversion rotation period $T_r = 1/f_r$, whose minimum value is the switching period T_s. For $V_{AB}(t)$, $m(t)$ switches between +1 and −1 within one period T_r.

According to the modulation property of the Fourier transform (convolution in frequency domain):

$$\mathcal{F}\{P_C(t)\} = \mathcal{F}\{m(t) \cdot P_B(t)\} = \mathcal{F}\{m(t)\} * \mathcal{F}\{P_B(t)\} \tag{16}$$

here, $*$ denotes the convolution operation. Among these, $\mathcal{F}\{P_B(t)\}$ is a series of discrete spectral lines $\sum C_n \delta(f - nf_s)$ located at nf_s; the spectrum of $\mathcal{F}\{m(t)\}$ is a discrete spectrum centered at the rotation frequency f_r and its harmonics: $\sum M_k \delta(f - kf_r)$.

Performing the convolution operation $\sum M_k \delta(f - kf_r) * \sum C_n \delta(f - nf_s)$ yields:

$$\mathcal{F}\{P_C(t)\} = \sum_n \sum_k M_k C_n \delta(f - (nf_s + kf_r)) \tag{17}$$

In Mode B, the disturbance energy is entirely concentrated at the frequency points nf_s. In Mode C, each discrete spectral line that was at nf_s in Mode B is "spread" into a comb-like spectrum cluster centered at nf_s with a spacing of f_r. Although the total energy (sum of squares of all sideband amplitudes) might remain approximately equal, the peak harmonic amplitude is significantly reduced. This process of "smearing" energy from discrete spectral lines into continuous sidebands effectively smoothens the harmonic spectrum. In our research case, the motor rotational frequency (fundamental frequency) is 346.667 Hz (period 2.885 ms). Selecting a reversal period of 150 μs means that the reversal action occurs approximately 60 times (3 * 2.885 ms/0.15 ms) within one fundamental cycle. This ensures that the harmonic dispersion effect can fully and uniformly develop over the entire fundamental cycle, thereby effectively smoothing the harmonics.

On the other hand, if the switching frequency f_s = 20 kHz. Setting $T_r \geq 3T_s$ is to satisfy the time required for phases A, B, and C to complete one full reversal sequence, which is exactly $3T_s$. A smaller T_r results in a more pronounced harmonic diffusion effect but also leads to a corresponding increase in switching loss. In this case, the system has a relatively high fundamental frequency, so a smaller T_r is selected to ensure effective harmonic dispersion. A typical SVPWM involves 6 switching operations per three cycles (each turn-on or turn-off of a switch counts as one operation). Building upon this alternating switching frequency, AI-SVPWM involves 8 switching operations per three cycles. This elevated switching activity consequently leads to a proportional rise in switching losses, which constitutes a fundamental trade-off between harmonic performance improvement and power conversion efficiency in the proposed methodology.

The implementation of AI-SVPWM is more complex. AI-SVPWM is no longer a single fixed sequence but involves switching between multiple predefined CMV-reducing sequences; specifically, it requires real-time inversion of the switching actions of different phases.

4 Simulation Verification

To compare the performance of the traditional SVPWM control strategy, the common-mode voltage suppression strategies AZSPWM1 and AZSPWM3, and the proposed I-SVPWM and AI-SVPWM in terms of output waveform characteristics, control performance, and common-mode voltage suppression capability, a simulation study was conducted using MATLAB/Simulink. Detailed simulation parameters are listed in Table 2, and the AI-SVPWM simulation module is illustrated in Fig. 8. The simulation results of the five control strategies are shown in Figs. 9–12.

Table 2: Simulation parameters

Parameters	Value	Parameters
DC voltage	V	270
Stator resistance (R_s)	Ω	0.045
Number of pole pairs (n_p)	pairs	2
q-axis inductance (L_q)	H	0.45e−3
d-axis inductance (L_d)	H	0.45e−3
Rotor PM flux (ψ_r)	Wb	0.0328
Rotational inertia (J)	kg·m^2	2.56e−4
Nominal torque	Nm	4.71
Nominal speed	rpm	10,400
switching frequency	kHz	20

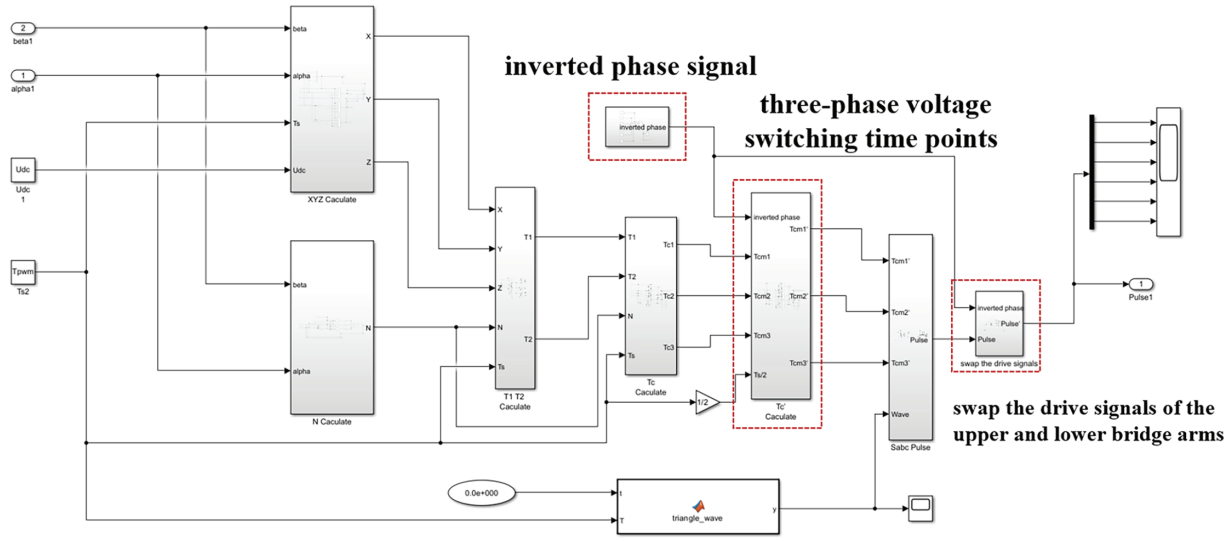


Figure 8: AI-SVPWM simulation model

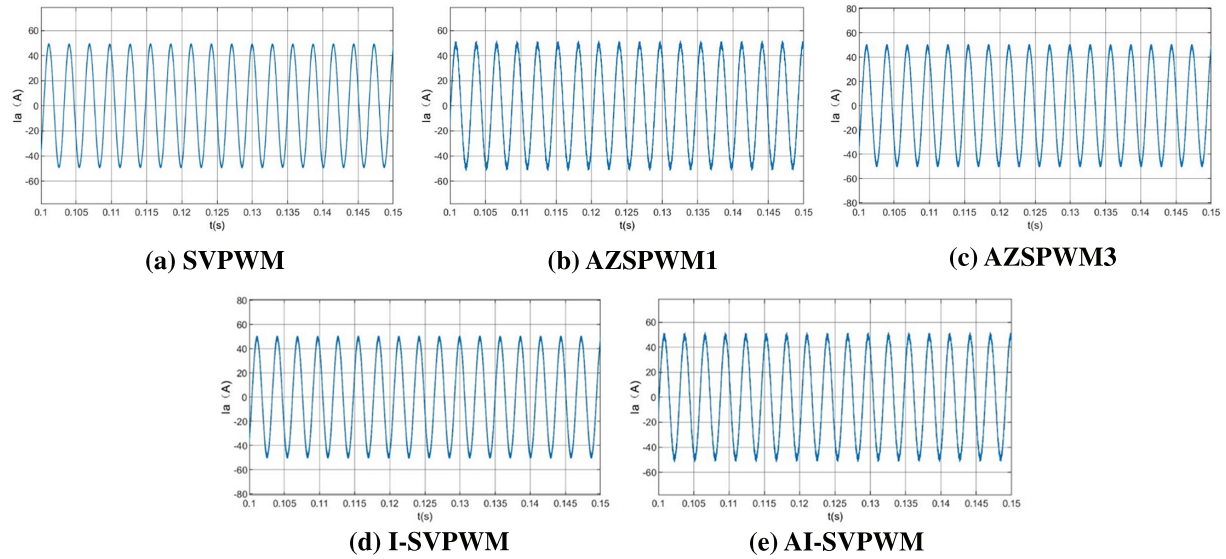
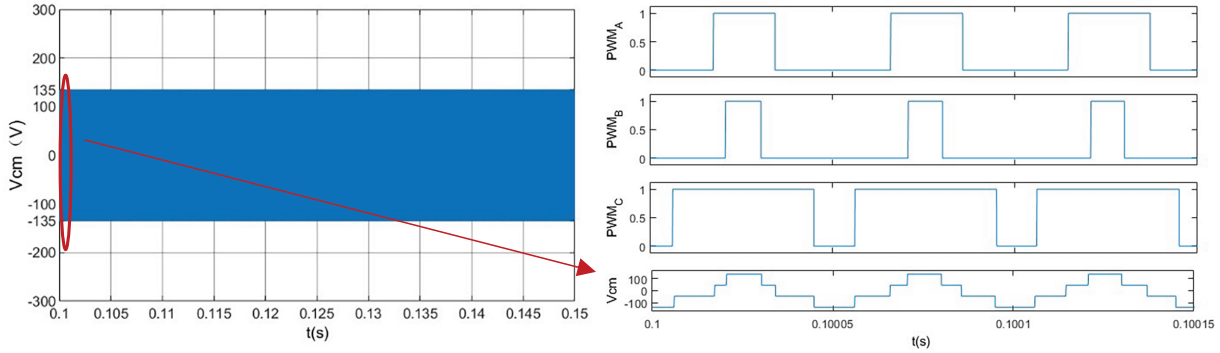
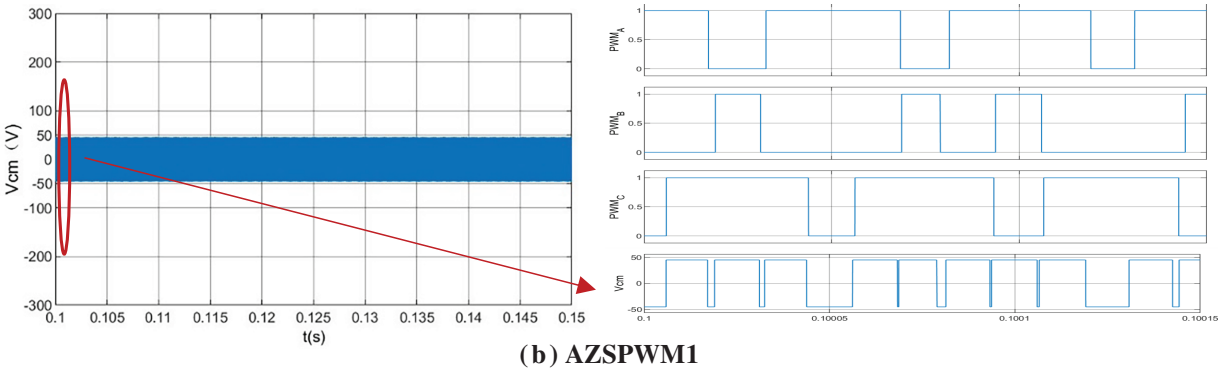


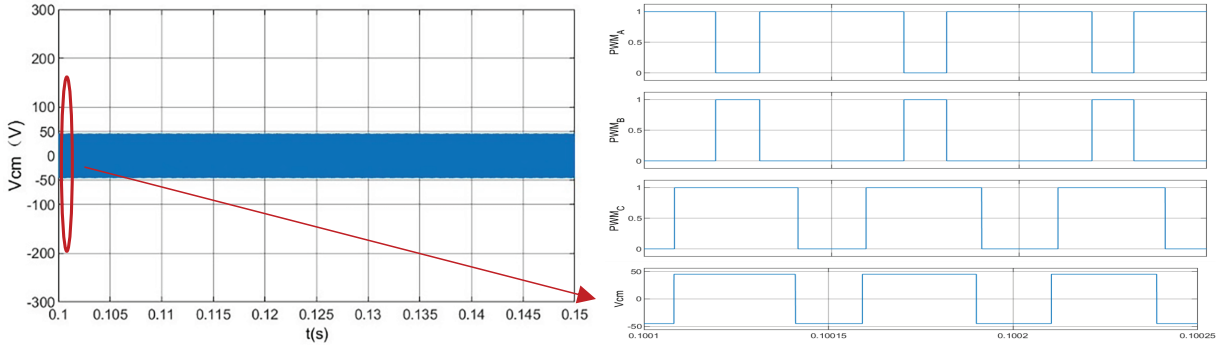
Figure 9: Phase A current comparison for different control strategies



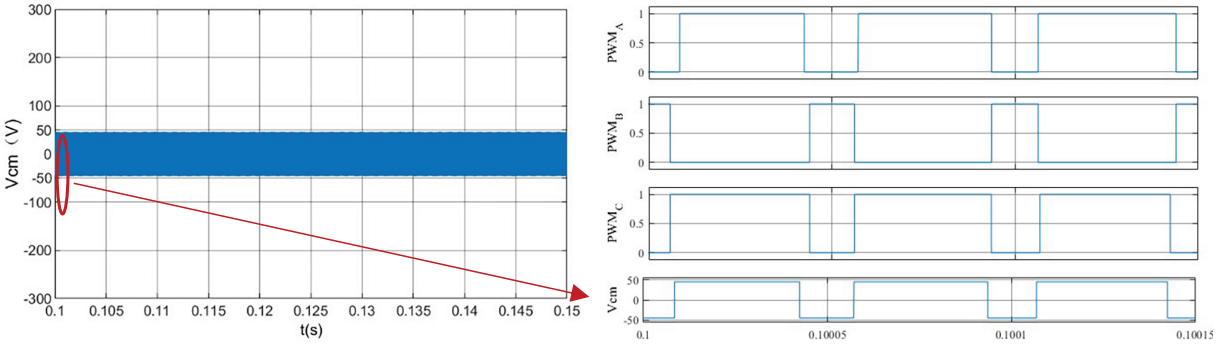
(a) SVPWM



(b) AZSPWM1

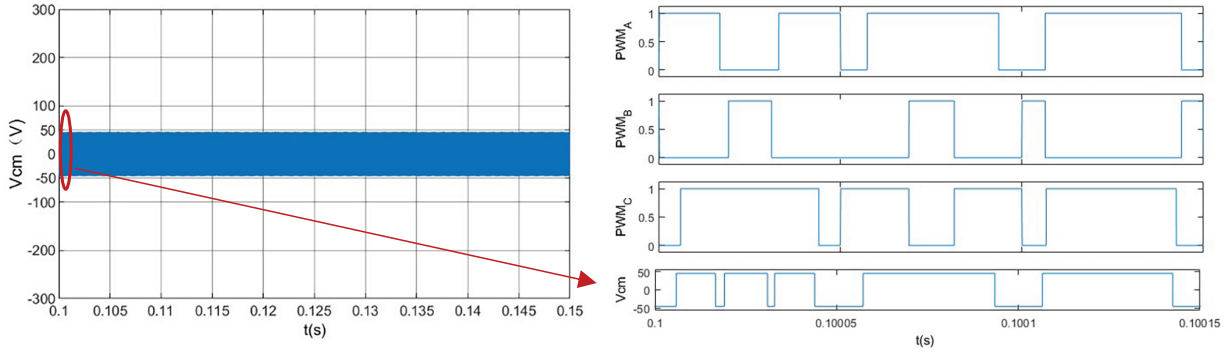


(c) AZSPWM3



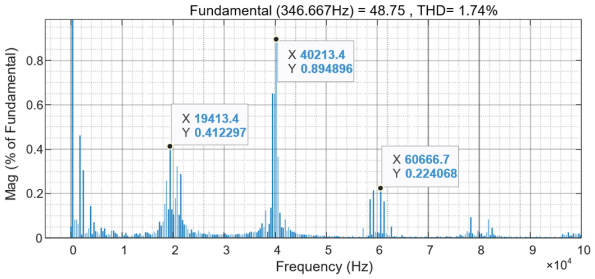
(d) I-SVPWM

Figure 10: (Continued)

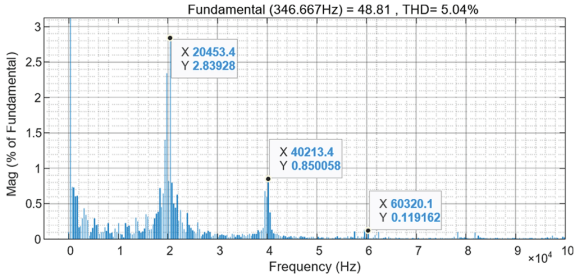


(e) AI-SVPWM

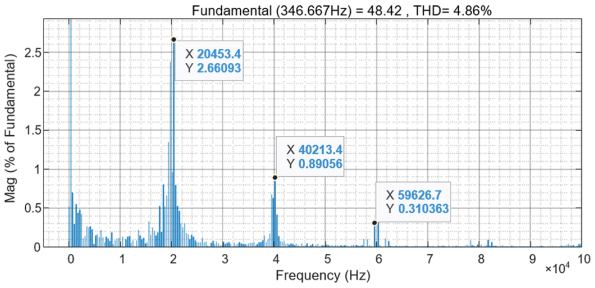
Figure 10: Common-mode voltage suppression comparison for different control strategies



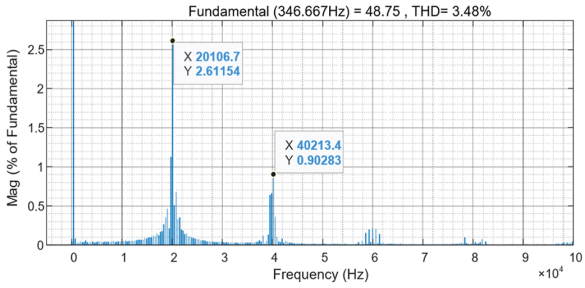
(a) SVPWM



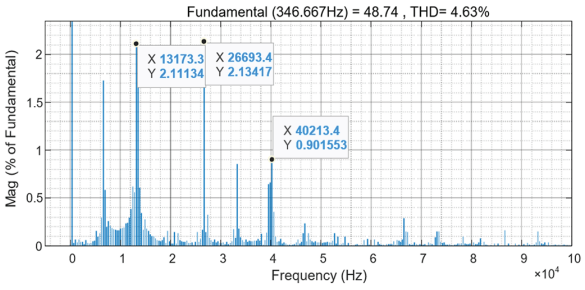
(b) AZSPWM1



(c) AZSPWM3



(d) I-SVPWM



(e) AI-SVPWM

Figure 11: FFT analysis comparison of phase current for different control strategies

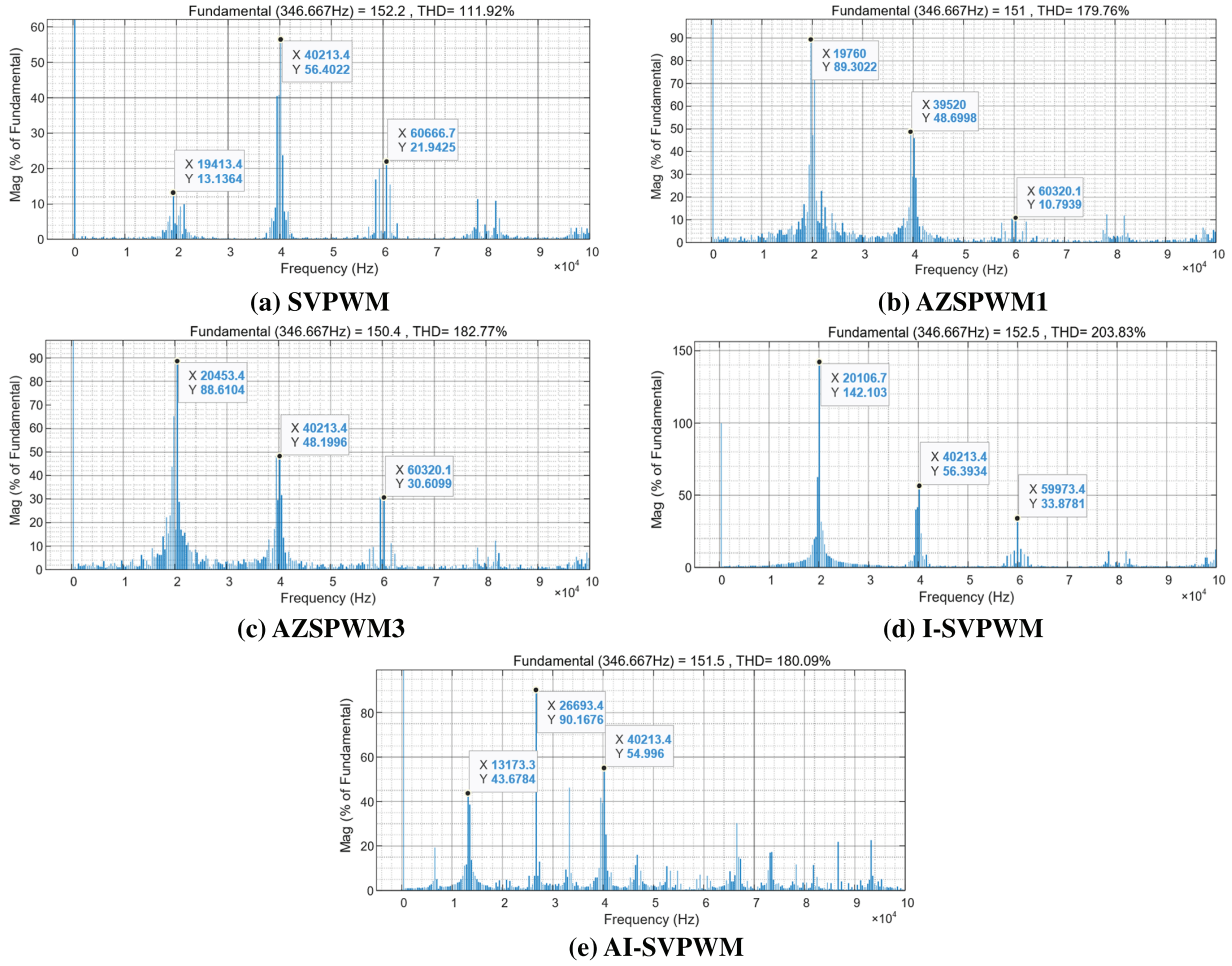


Figure 12: FFT analysis comparison of line voltage for different control strategies

Fig. 9 shows the phase A current waveforms in the time domain. It can be observed that the traditional SVPWM exhibits slightly superior waveform quality compared to the four common-mode voltage suppression strategies. Nevertheless, no significant distortion is observed in the phase current waveforms of the four common-mode voltage suppression strategies, and their performance remains adequate for general application requirements.

As shown in Fig. 10, the common-mode voltage waveforms are compared in the time domain. The conventional SVPWM produces a CMV with the largest fluctuation, swinging between –135 and +135 V. By comparison, both I-SVPWM and the proposed AI-SVPWM confine the CMV variation within a significantly reduced range of –45 to +45 V.

The total harmonic distortion (THD) analysis of the phase currents in Fig. 11 reveals that the elimination of zero vectors leads to varying degrees of THD increase in all four common-mode voltage suppression strategies. However, the proposed I-SVPWM and AI-SVPWM exhibit lower THD compared to the two conventional strategies, AZSPWM1 and AZSPWM3. The harmonic spectrum of I-SVPWM exhibits noticeable high-order discrete harmonics; for example, the component at 20,106.7 Hz reaches 2.61% of the fundamental component. Although the overall THD of AI-SVPWM is higher than that of I-SVPWM, the spectral

spreading effect helps reduce the highest harmonic amplitude to only 2.11% of the fundamental, which is beneficial in alleviating audible noise and structural vibration at specific frequencies.

Fig. 12 presents the THD analysis of the line voltage. Among the five methods, I-SVPWM shows the worst harmonic performance. In comparison, the proposed AI-SVPWM reduces the total THD from 203.83% to 180.09% and lowers the maximum harmonic amplitude from 142% to 90%, thereby partly suppressing the most severe harmonic concentration. A detailed comparison of each modulation method is presented in Table 3.

Table 3: Performance comparison of different common-mode voltage suppression strategies

Strategy	Line current harmonic content	Phase voltage harmonic content	Line current harmonic amplitude	Phase voltage harmonic amplitude	Switching loss	CMV amplitude
SVPWM	1.74%	111.92%	0.89%	56.40%	No effect	±135
AZSPWM1	5.04%	179.76%	2.84%	89.30%	Rise modestly	±45
AZSPWM3	4.86%	182.77%	2.66%	88.61%	No effect	±45
I-SVPWM	3.48%	203.83%	2.61%	142.10%	No effect	±45
AI-SVPWM	4.63%	180.09%	2.13%	90.17%	Rise	±45

5 Conclusion

Through theoretical derivation and simulation, this paper analyzes the mechanism of common-mode voltage (CMV) suppression in I-SVPWM and AI-SVPWM strategies, as well as the high-frequency harmonic dispersion principle in AI-SVPWM. Simulation results indicate that traditional SVPWM provides benchmark optimal waveform quality, but its high CMV magnitude is an inherent drawback. AZSPWM3 and I-SVPWM achieve effective CMV suppression without increasing switching losses, making them excellent choices that balance efficiency and reliability. Among them, I-SVPWM is more conducive to obtaining smooth motor currents compared to AZSPWM1 and AZSPWM3. AI-SVPWM, to some extent, suppresses the high-frequency harmonic amplitudes of phase currents and line voltages, but at the cost of increased switching losses. This trade-off requires careful evaluation in ultra-high switching frequency or high-power applications.

The final strategy selection should be based on a comprehensive consideration of the specific application's requirements for current quality, voltage quality, system efficiency, and electromagnetic compatibility. For applications pursuing ultimate current waveform quality (such as ultra-high-precision servo systems), traditional SVPWM may still be the preferable choice.

However, for applications where system reliability, longevity, and low EMI are prioritized (such as electric vehicle powertrains, aerospace systems, data center cooling, and industrial spindle drives), the potential hazards posed by CMV can be critical and costly. In these scenarios, trading a controlled and limited degradation in current waveform quality (e.g., THD increasing from 1.74% to around 4%) for a substantial improvement in system reliability and safety (e.g., a 66.7% reduction in CMV) represents a highly worthwhile engineering compromise.

Acknowledgement: This research was supported by Beijing Research Institute of Precise Mechanics and Controls. The author expresses sincere gratitude to all those who participated in this study.

Funding Statement: This study is supported by the Open Fund of Innovation Center for Control Actuators.

Author Contributions: The authors confirm contribution to the paper as follows: study conception, task division, content planning, simulation validation, and draft manuscript preparation: Meng Zhang, Jie Zhang; project introduction, progress and direction oversight, funding acquisition, and final manuscript review: Lijuan Zhang, Shiliang Miao, Jiangong Yang; data support, and final manuscript review: Yajun Zhao, Feifei Bu. All authors reviewed and approved the final version of the manuscript.

Availability of Data and Materials: The authors confirm that the data used in this study are available on request. Data supporting this study are included in the article.

Ethics Approval: Not applicable.

Conflicts of Interest: The authors declare no conflicts of interest to report regarding the present study.

Abbreviations

SVPWM	Space Vector Pulse Width Modulation
I-SVPWM	Inverted SVPWM
AI-SVPWM	Alternating Inverted SVPWM
PMSM	Permanent Magnet Synchronous Motors
RSPWM	Remote State PWM
NSPWM	Near State PWM
AZSPWM	Active Zero State PWM
EMI	Electromagnetic Interference
THD	Total Harmonic Distortion

References

1. Singh B, Murshid S. A grid-interactive permanent-magnet synchronous motor-driven solar water-pumping system. IEEE Trans Ind Appl. 2018;54(5):5549–61. doi:10.1109/tia.2018.2860564.
2. Zhu D, Zhao Y, Ai D, Zhang L, Zhou Y. Efficiency optimization of PMSM in flywheel energy storage under multiple working conditions based on genetic algorithm. Energy Storage Sci Technol. 2024;13(10):3582–92. doi:10.1109/iccepe62686.2024.10931709.
3. Wang Z, Ching TW, Huang S, Wang H, Xu T. Challenges faced by electric vehicle motors and their solutions. IEEE Access. 2021;9:5228–49. doi:10.1109/access.2020.3045716.
4. Mohammed HS, Sabry AH, Hameed HK, Uğurenver A. Impact of pulse-width modulation techniques on inverter efficiency and motor current quality in permanent-magnet synchronous motor drives: a simulation study. Measurement. 2026;258(7):119107. doi:10.1016/j.measurement.2025.119107.
5. Bu F, Ma B, Du R, Sun T, Chu J, Liu Q, et al. Multiaverage random switching frequency space vector pulsewidth modulation strategy for high-order harmonics dispersion. IEEE J Emerg Sel Top Power Electron. 2023;11(4):4010–21. doi:10.1109/jestpe.2023.3266491.
6. Chen X, Liu H, Zhang D, Zhang X. Research on the influence of shaft current on E-motor electromagnetic interference test results. In: Proceedings of the 2020 IEEE 3rd International Conference on Information Systems and Computer Aided Education (ICISCAE); 2020 Sep 27–29; Dalian, China. p. 56–61. doi:10.1109/iciscae51034.2020.9236793.
7. Agrawal S, Kanchan RS. Carrier phase shift modulation for reducing the common mode voltage in a two-level three-phase inverter. In: Proceedings of the IECON 2018—44th Annual Conference of the IEEE Industrial Electronics Society; 2018 Oct 21–23; Washington, DC, USA. p. 1067–72. doi:10.1109/IECON.2018.8591776.
8. Morya AK, Gardner MC, Anvari B, Liu L, Yepes AG, Doval-Gandoy J, et al. Wide bandgap devices in AC electric drives: opportunities and challenges. IEEE Trans Transp Electrif. 2019;5(1):3–20. doi:10.1109/tte.2019.2892807.

9. ECE R10 06. Uniform provisions concerning the approval of vehicles with regard to electromagnetic compatibility, 06 series of amendments to UN Regulation No.10: ECE R10 06. Geneva, Switzerland: UNECE; 2019.
10. Liu D, Xiong S, Song Z, Qiu H. Review of harmonic suppression technology based on photovoltaic grid-connected inverter. J Electr Eng. 2025;20(6):223–38. (In Chinese).
11. von Jouanne A, Dai S, Zhang H. A multilevel inverter approach providing DC-link balancing, ride-through enhancement, and common-mode voltage elimination. IEEE Trans Ind Electron. 2002;49(4):739–45. doi:10.1109/TIE.2002.801233.
12. Chen T, Xiao H, Cheng M. Three-phase ZVS-TNPC inverter with common-mode voltage suppression. IEEE Trans Power Electron. 2025;40(12):18350–64. doi:10.1109/tpel.2025.3591439.
13. Aghaei H, Babaei E, Sharifian MBB, Iqbal A. Dual three-phase sparse inverter: topology analysis, PWM scheme, and common mode voltage elimination. IEEE Open J Ind Electron Soc. 2025;6:1398–422. doi:10.1109/ojies.2025.3599409.
14. Zhong Z, Wang Q, Yin X. Performance comparison of common-mode voltage suppression of different space vector modulation algorithms. Electr Mach Control Appl. 2021;48(5):26–33. (In Chinese).
15. Hava AM, Ün E. A high-performance PWM algorithm for common-mode voltage reduction in three-phase voltage source inverters. IEEE Trans Power Electron. 2011;26(7):1998–2008. doi:10.1109/TPEL.2010.2100100.
16. Seo S, Kim S, Shin HJ, Lee C, Lee JS. Reduced common mode voltage PWM strategy with optimized switching sequence for three phase motor drives. IEEE Access. 2025;13:188702–12. doi:10.1109/ACCESS.2025.3625755.
17. Hava AM, Ün E. Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters. IEEE Trans Power Electron. 2009;24(1):241–52. doi:10.1109/TPEL.2008.2005719.
18. Tallam RM, Kerkman RJ, Leggate D, Lukaszewski RA. Common-mode voltage reduction PWM algorithm for AC drives. IEEE Trans Ind Appl. 2010;46(5):1959–69. doi:10.1109/tia.2010.2057396.
19. Cacciato M, Consoli A, Scarcella G, Testa A. Reduction of common-mode currents in PWM inverter motor drives. IEEE Trans Ind Appl. 1999;35(2):469–76. doi:10.1109/28.753643.
20. Un E, Hava AM. A near-state PWM method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters. IEEE Trans Ind Appl. 2009;45(2):782–93. doi:10.1109/TIA.2009.2013580.
21. Chen H, Zhao H. Review on pulse-width modulation strategies for common-mode voltage reduction in three-phase voltage-source inverters. IET Power Electron. 2016;9(14):2611–20. doi:10.1049/iet-pel.2015.1019.
22. Hou CC, Shih CC, Cheng PT, Hava AM. Common-mode voltage reduction modulation techniques for three-phase grid connected converters. In: Proceedings of the 2010 International Power Electronics Conference—ECCE ASIA; 2010 Jun 21–24; Sapporo, Japan. p. 1125–31. doi:10.1109/IPEC.2010.5543223.
23. Leng Y, Zhu R, Hoeher PA, Liserre M. DC-AC talkative power conversion based on variable zero-vector position modulation. IEEE Trans Power Electron. 2025;40(6):7954–66. doi:10.1109/tpel.2025.3541040.
24. Khan AA, Zaffar NA, Ikram MJ, Wu Y, Peretti L. Combined reduction of DC-link harmonics and common mode voltage in interleaved multi-inverter systems by modified SVPWM schemes. IEEE Trans Ind Electron. 2025;72(5):4364–74. doi:10.1109/TIE.2024.3476937.
25. Huang H, Zhang W, Xu Y, Zhang H, Zou J. A method for PWM frequency harmonic suppression using zero-vector switching SVPWM strategy in three-level inverter drive systems. IEEE J Emerg Sel Top Power Electron. 2025;13(2):1482–91. doi:10.1109/JESTPE.2024.3485962.
26. Long G, Qian F, Huang W, Ge Z. Zero-vector allocation of SVPWM in shunt-type APF. Telecom Power Technol. 2016;33(01):42–4. (In Chinese).
27. Tawfiq KB, Zeineldin H, Al-Durra A, El-Saadany EF. Enhanced SVPWM techniques for six-phase inverters: mitigation of current harmonics and common mode voltage. IEEE Open J Ind Electron Soc. 2024;5:1339–52. doi:10.1109/OJIES.2024.3512588.
28. Sabry AH, Mohammed ZM, Nordin FH, Nik Ali NH, Al-Ogaili AS. Single-phase grid-tied transformerless inverter of zero leakage current for PV system. IEEE Access. 2020;8:4361–71. doi:10.1109/ACCESS.2019.2963284.