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ARTICLE

A Coordinated Multi-Loop Control Strategy for Fault Ride-Through in Grid-Forming Converters

Zhuang Liu[#], Mingwei Ren, Kai Shi[*] and Peifeng Xu

Department of Electrical Engineering, Jiangsu University, Zhenjiang, 21200, China

*Corresponding Author: Kai Shi. Email: xshikai@ujs.edu.cn

[#]Frist Author: Zhuang Liu

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ABSTRACT: Grid-Forming (GFM) converters are prone to fault-induced overcurrent and power angle instability during grid fault-induced voltage sags. To address this, this paper develops a multi-loop coordinated fault ride-through (FRT) control strategy based on a power outer loop and voltage-current inner loops, aiming to enhance the stability and current-limiting capability of GFM converters during grid fault conditions. During voltage sags, the GFM converter's voltage source behavior is maintained by dynamically adjusting the reactive power reference to provide voltage support, thereby effectively suppressing the steady-state component of the fault current. To address the active power imbalance induced by voltage sags, a dynamic active power reference correction method based on apparent power is designed to mitigate power angle oscillations and limit transient current. Moreover, an adaptive virtual impedance loop is implemented to enhance dynamic transient current-limiting performance during the fault initiation phase. This approach improves the responsiveness of the inner loop and ensures safe system operation under various fault severities. Under asymmetric fault conditions, a negative-sequence reactive current compensation strategy is incorporated to further suppress negative-sequence voltage and improve voltage symmetry. The proposed control scheme enables coordinated operation of multiple control objectives, including voltage support, current suppression, and power angle stability, across different fault scenarios. Finally, MATLAB/Simulink simulation results validate the effectiveness of the proposed strategy, showcasing its superior performance in current limiting and power angle stability, thereby significantly enhancing the system's fault ride-through capability.

KEYWORDS: Grid-forming converter; multi-loop coordination; negative-sequence control; fault ride-through

1 Introduction

With the full-scale progression advancement of the energy transition and the high penetration of renewable energy generation coupled with power electronic devices, the traditional centralized power system architecture dominated by synchronous generators (SGs) is undergoing a structural transformation towards a diversified paradigm characterized by the coexistence of distributed microgrids and large-scale renewable energy plants [1,2]. SGs can inherently counteract grid disturbances through prime mover governor systems and rotor inertia dynamics, maintaining grid stability, whereas distributed generation (DG) systems lack such inherent capabilities due to the absence of rotating masses and electromechanical control mechanisms [3]. To improve system stability and robustness under high renewable energy penetration, GFM converters have emerged as a pivotal solution and experienced rapid technological advancement [4].

In grid-connected operation, GFM converters leverage their inherent voltage source behavior to independently establish and regulate grid voltage and frequency, thereby ensuring stable operation under weak grid conditions [5]. However, due to the limitations of power electronic devices in short-circuit current withstand capability, it is urgent to implement effective output current limiting strategies during faults to enhance FRT capability. Currently, the main current limiting strategies for GFM converters include mode switching, power regulation, direct modification of voltage reference, and virtual impedance [6,7].

The mode-switching strategy proposed in [8,9] switches the converter from GFM to grid-following (GFL) control during grid faults. Unfortunately, this approach abandons the inherent voltage and frequency support capabilities of GFM converters, which can compromise grid stability under high renewable penetration. In contrast to mode-switching strategies, power regulation strategies have been extensively utilized in FRT of single GFM converters. In [10], active power commands are dynamically adjusted and virtual resistance is configured to mitigate power imbalance and stabilize the power angle. However, voltage support during faults is not considered, making it unsuitable for high-penetration scenarios. To enhance voltage support capability, Ref. [11] introduces a reactive power compensation based on grid-side voltage deviation, while Ref. [12] incorporates a second-order transient voltage component into the reactive power-voltage control loop to improve the voltage source behavior of GFM converters. However, these methods fail to address power angle deviation issues, and exhibit limited effectiveness in fault current limiting. To resolve these challenges, Refs. [13–15] propose a coordinated control of active and reactive power to provide voltage support while suppressing power angle deviation. Furthermore, Refs. [16,17] enhance FRT capability by dynamically compensating angular frequency and adjusting voltage references, thereby improving both angle stability and voltage support.

The aforementioned control strategies mainly focus on symmetrical faults. For more common and complex asymmetrical faults, Ref. [18] adopts αβ-frame control of voltage and current, avoiding dq-coordinate transformation to improve dynamic response and more intuitively reflect grid asymmetry and harmonic characteristics. However, this method exhibits weak current decoupling capability and limited control accuracy and steady-state performance. To overcome these limitations, Refs. [19,20] directly modify the voltage reference values and incorporate virtual impedance control to effectively suppress fault current during asymmetrical faults.

In complex grid conditions, GFM inverters need to simultaneously address both symmetrical and asymmetrical faults to ensure reliable FRT capability, yet existing research on this respect remains insufficient. To bridge this gap, Ref. [21] integrates virtual impedance with and model predictive control to limit fault current, while Ref. [22] combines adaptive virtual admittance with power loop freezing. Though effective in current control, both approaches neglect reactive voltage support and power angle stability, leading to compromised capability in dynamically regulating fault currents within ideal limits.

Current FRT control strategies typically focus on either symmetrical or asymmetrical faults individually, lacking a unified approach for handling different fault types. In the context of increasing penetration of both renewable energy and power electronic devices, a coordinated inner- and outer-loop control strategy is proposed to enhance the system's stability and ride-through capability under various fault conditions, while also improving its support for grid voltage and frequency. The main contributions are as follows:

1) A dynamic power reference adjustment method is proposed, which adjust the power setpoint based on the depth of voltage sags and the inverter's apparent power rating, limiting fault overcurrent and improving system dynamic stability.

2) A dual second-order generalized integrator (DSOGI) based sequence decomposition is employed to decouple fault current and voltage into positive and negative components. An adaptive virtual impedance

model is constructed in the positive sequence inner loop, with current limiting to precisely regulate the fault current magnitude.

3) In response to inverter negative-sequence current control requirements [23], a novel dual-loop negative-sequence voltage-current regulation strategy is proposed. This strategy implements coordinated control of negative-sequence voltage and current to achieve reactive current compensation, suppress negative-sequence voltage, and reduce grid voltage asymmetry.

The rest of this paper is organized as follows. Section 2 delineates the main circuit and control strategy of the GFM Converter. Section 3 elaborates critical technical challenges encountered during faults. Section 4 presents the FRT control strategy with adaptive current-limiting mechanisms. Section 5 conducts simulation analysis for different fault types. Section 6 concludes this paper by summarizing key findings and discussing their engineering implications for renewable-integrated power systems.

2 Topology and Control Strategies for GFM Converter

During grid faults, GFM converters can provide voltage and frequency support, thereby enhancing transient stability and fault ride-through capability in weak grids. When combined with virtual synchronous generator (VSG) control, GFM converters can further improve system damping and inertia, demonstrating significant potential for ensuring secure and reliable operation.

2.1 The Main Architecture of GFM Converters

The system structure of a GFM grid-connected inverter is shown in Fig. 1, where U_{dc} represents the DC-side voltage, and $Q1$–$Q6$ are the power switches (IGBTs) controlled by gate signals to perform the inversion process. The L_f–C_f filter is used to attenuate high-frequency noise and harmonics, thereby improving inverter performance and efficiency. V_{abc} and I_{abc} represent the voltage and current at the point of common coupling (PCC), respectively. R_f denotes the equivalent resistance between the inverter and the PCC. L_g and R_g represent the equivalent inductance and resistance of the grid-side line, respectively. U_g denotes the corresponding grid-side voltage.

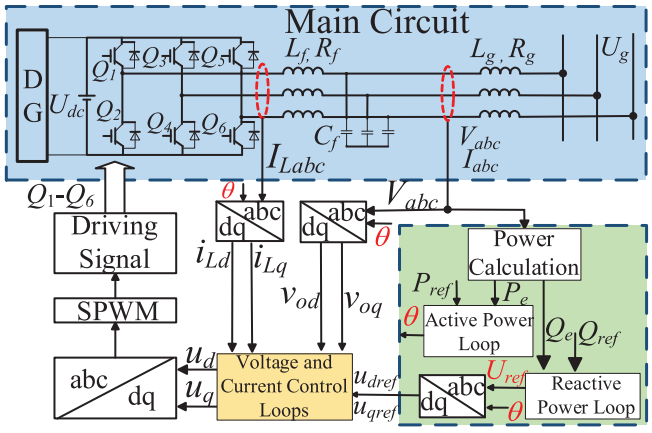

Figure 1: System structure of a GFM grid-connected converter

During the operation of a grid-forming converter, the DC power generated by distributed energy sources is converted into AC power through an inverter, with its core control based on the VSG strategy. The VSG controller first acquires the voltage and current at the PCC, and then calculates the active power P_e and

reactive power Q_e via a power computation module. Based on this, it generates a reference voltage U_{ref} and phase angle θ.

Subsequently, a Park transformation is applied to convert the three-phase signals U_{ref}, V_{abc} and I_{abc} from the stationary abc frame to the synchronous rotating dq0 frame, resulting in steady-state DC quantities. This facilitates simpler and more efficient control. The resulting dq components are fed into a dual-loop voltage and current control structure, enabling precise regulation of the inverter's output.

Finally, an inverse Park transformation is used to reconstruct the three-phase sinusoidal reference signals. Sinusoidal Pulse Width Modulation (SPWM) is then employed to generate modulation waves and corresponding gate signals to control the switching states of power devices such as IGBTs. This process efficiently achieves DC-AC conversion, and the output is filtered through an LC filter before being delivered to the grid.

2.2 Control Strategy of VSG

The VSG control loop mainly consists of two control layers. The first part is the outer power loop, where the active loop emulates the inertia and frequency modulation characteristics of SG, and the reactive loop stabilizes the output voltage by adjusting reactive power [24]. The corresponding control equations are given in Eq. (1) as follows.

$$\begin{cases} P_{ref} - P_e - D_p\left(\omega - \omega_n\right) = J\omega_n \dfrac{d\omega}{dt} \\ Q_{ref} - Q_e - D_q\left(V - V_n\right) = K\dfrac{dE_m}{dt} \end{cases} \tag{1}$$

where P_{ref} and P_e, as well as Q_{ref} and Q_e, respectively, represent the reference and actual values of active and reactive power. D_p and D_q respectively denote the damping factor and the reactive power-voltage droop coefficient. J represents the equivalent virtual moment of inertia, while K is the inertia control coefficient, ω and ω_n represent the real-time angular frequency and its rated value, respectively, while V and V_n correspond to the current output voltage and the rated voltage, E_m denotes the amplitude of the virtual armature electromotive force (EMF).

The second part is the inner voltage-current loop, which enables precise fault current regulation during FRT. As the LC filter forms a second-order system, the dual-loop control architecture enhances damping, suppresses resonance, and improves stability and response [25]. The voltage outer loop employs a PI controller to generate reference current signals, which are subsequently tracked by the current inner loop to regulate power flow. Eqs. (2) and (3) respectively represent the voltage and current loop control equations.

$$\begin{cases} i_{dref} = \left(u_{dref} - v_{od}\right) * \left(k_{pu} + \dfrac{k_{iu}}{s}\right) - \omega C_f v_{oq} \\ i_{qref} = \left(u_{qref} - v_{oq}\right) * \left(k_{pu} + \dfrac{k_{iu}}{s}\right) - \omega C_f v_{od} \end{cases} \tag{2}$$

$$\begin{cases} u_d = v_{od} + \left(i_{dref} - i_{Ld}\right) * \left(k_{pi} + \dfrac{k_{ii}}{s}\right) + \omega L_f i_{Lq} \\ u_q = v_{oq} + \left(i_{qref} - i_{Lq}\right) * \left(k_{pi} + \dfrac{k_{ii}}{s}\right) + \omega L_f i_{Ld} \end{cases} \tag{3}$$

2.3 Positive and Negative Sequence Separation under Asymmetrical Faults

A three-phase three-wire system is used, where only positive and negative sequence components exist under asymmetrical faults. To achieve precise control, voltage and current signals must undergo positive-negative sequence decomposition, with negative sequence current regulated. As illustrated in Fig. 2, the DSOGI method for second-order filtering effectively extracts positive- and negative-sequence components., enhancing system stability and robustness against disturbances. Specifically, 3S/2S corresponds to the Clarke transformation, 2S/2R corresponds to the αβ–dq transformation, and K_{so} denotes the proportional gain. Eq. (4) defines the transfer function of the SOGI, where $D(s)$ and $Q(s)$ correspond to the band-pass and low-pass filter structures, respectively [26].

$$\begin{cases} D(s) = \dfrac{v'(s)}{v(s)} = \dfrac{K_{so}\omega s}{s^2 + K_{so}\omega s + \omega^2} \\ Q(s) = \dfrac{qv'(s)}{v(s)} = \dfrac{K_{so}\omega s}{s^2 + K_{so}\omega s + \omega^2} \end{cases} \tag{4}$$

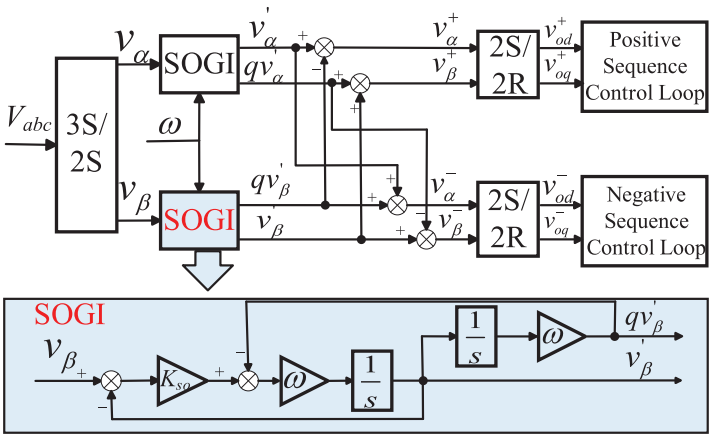

Figure 2: Overall control block diagram of DSOGI

3 Transient Response Characteristics of VSG to Grid Faults

3.1 Power Angle Characteristics

The power angle δ serves as a key indicator for evaluating the transient stability of VSGs. Post-fault system stability is determined by whether δ remains within a bounded range. Divergence of δ will lead to instability. δ represents the phase difference between inverter's voltage $E\angle\delta$ and grid voltage $U_g\angle 0°$, as mathematically defined Eq. (5).

$$\delta = \int (\omega - \omega_n)\, dt \tag{5}$$

The active and reactive power outputs of the converter are expressed by Eqs. (6) and (7), respectively.

$$P_e = \frac{3}{2}\frac{EU_g \sin\delta}{X_g} \tag{6}$$

$$Q_e = \frac{E\left(E - U_g\cos\delta\right)}{X_g} \tag{7}$$

Based on Eq. (6), the VSG power angle curve is plotted in Fig. 3, where curve I represents the pre-fault curve and curve II denotes the post-fault curve. The power angle variation during the fault is as follows:

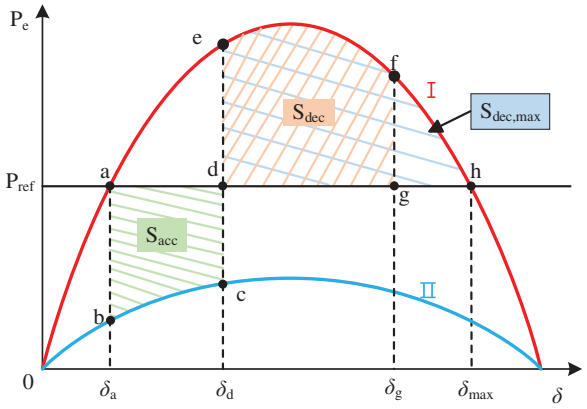

Figure 3: Power angle curve of the GFM converter

① **Normal Operation Stage:** The output power $P_e = P_{ref}$, and the power angle is δ_a, corresponding to operating point *a*.

② **Fault Occurrence Stage:** The output power P_e decreases, the power-angle curve shifts from region I to region II, and the operating point moves from *a* to *b*.

③ **Acceleration Stage:** As $P_{ref} > P_e$, under the action of the outer power control loop, $d\omega/dt > 0$, the power angle increases, and the operating point moves from *b* to *c*.

④ **Fault Clearance Instant:** The output power P_e increases, and the operating point shifts from *c* to *e*. The corresponding power angle δ_d is referred to as the *critical angle*, and the accumulated area is known as the *acceleration area* S_{acc}.

⑤ **Deceleration Stage:** As $P_{ref} < P_e$, under the continued influence of the power control loop, $d\omega/dt > 0$, the power angle keeps increasing, and the operating point moves from *e* to *f*. The accumulated area during this stage is called the *deceleration area* S_{dec}.

⑥ **Transient Stability Assessment:** If the power angle δ_g at point *f* does not exceed the maximum angle δ_{max} at point *h*, and the deceleration area S_{dec} does not exceed the maximum allowable deceleration area $S_{dec,max}$, the system is considered *transiently stable*. The operating point then returns from *f* to *a*, and stable operation is restored.

To ensure power angle stability, according to the *equal-area criterion*, the following condition must be satisfied: $S_{acc} \leq S_{dec} \leq S_{dec,max}$.

During grid faults that induce voltage sags, VSG's active power decreases, and the limited bandwidth of the power loop results in delayed response, causing transient δ deviation and instability. Although the excitation system exhibits rapid dynamic response characteristics, it fails to provide instantaneous compensation during abrupt voltage drops. Concurrently, the increased reactive power demand can lead to insufficient reactive power injection. Therefore, coordinated active power regulation and reactive power compensation must be implemented simultaneously [27].

3.2 Fault Current Characteristics

During grid faults, the GFM inverter operates as a voltage source, and its constant potential during the initial fault stage causes a sudden voltage discrepancy with the grid, triggering a rapid current surge

and active power imbalance. This results in δ expansion and fault overcurrent, threatening system stability. Consequently, coordinated control of δ and stringent fault current limitation are crucial. The equivalent circuit of the GFM inverter is shown in Fig. 4, where $u_{pcc(0-)}$ and $u_{pcc(0+)}$ respectively represent the grid voltage pre-fault and post-fault.

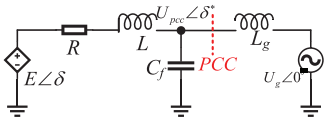

Figure 4: Power angle curve of the GFM converter

With reference to Fig. 4 and incorporating the resistive component of the system, the voltage current relationship can be derived based on Kirchhoff's Voltage Law (KVL), as shown in Eq. (8).

$$e(t) = Ri(t) + L\frac{di(t)}{dt} + u_{pcc}(t) \tag{8}$$

The output current injected into the grid before the occurrence of the voltage sag is given as follows:

$$i_{(0-)} = \frac{e - u_{pcc(0-)}}{R + j\omega L} \tag{9}$$

At the moment of the voltage sag, since the instantaneous voltage e of the converter remains unchanged, the instantaneous response of the fault current can be derived as follows:

$$i(t) = i_{(0-)} + \frac{u_{pcc(0-)} - u_{pcc(0+)}}{R + j\omega L}\left(1 - e^{-\frac{R}{L}t}\right) = \frac{u_{pcc(0+)} - u_{pcc(0-)}}{R + j\omega L}e^{-\frac{R}{L}t} + \frac{e - u_{pcc(0+)}}{R + j\omega L} \tag{10}$$

During a fault, the fault current exhibits different characteristics at different stages, mainly consisting of a transient component i_z and a steady-state component i_w [16]. Therefore, the fault current i_f of the GFM inverter can be expressed as:

$$\begin{cases} i_f = i_z + i_w \\ i_z = \dfrac{u_{pcc(0+)} - u_{pcc(0-)}}{R + j\omega L}e^{-\frac{R}{L}t} \\ i_w = \dfrac{e - u_{pcc(0+)}}{R + j\omega L} \end{cases} \tag{11}$$

During grid voltage sags, $u_{pcc(0+)}$ decreases. To suppress i_z, the equivalent impedance can be adjusted to reduce the linear part and accelerate the decay of the nonlinear part. When i_w increases, the steady-state component control is achieved by adjusting the equivalent impedance and power outer loop to control the internal potential.

4 Multi-Loop Coordinated Control Strategy for FRT

With the in-depth investigation of the FRT performance of GFM converters and the analysis of power angle and fault current characteristics, it is necessary to dynamically adjust the power reference in the outer power control loop during voltage sags caused by grid-side faults. Meanwhile, to suppress the increase in fault current, an adaptive virtual impedance is introduced into the inner control loop, enabling dynamic

coordination between the inner and outer loops. As shown in Fig. 5, the proposed control strategy aims to mitigate the δ deviation and fault current surge under various fault conditions, thereby ensuring the safe and reliable operation of the GFM converter system.

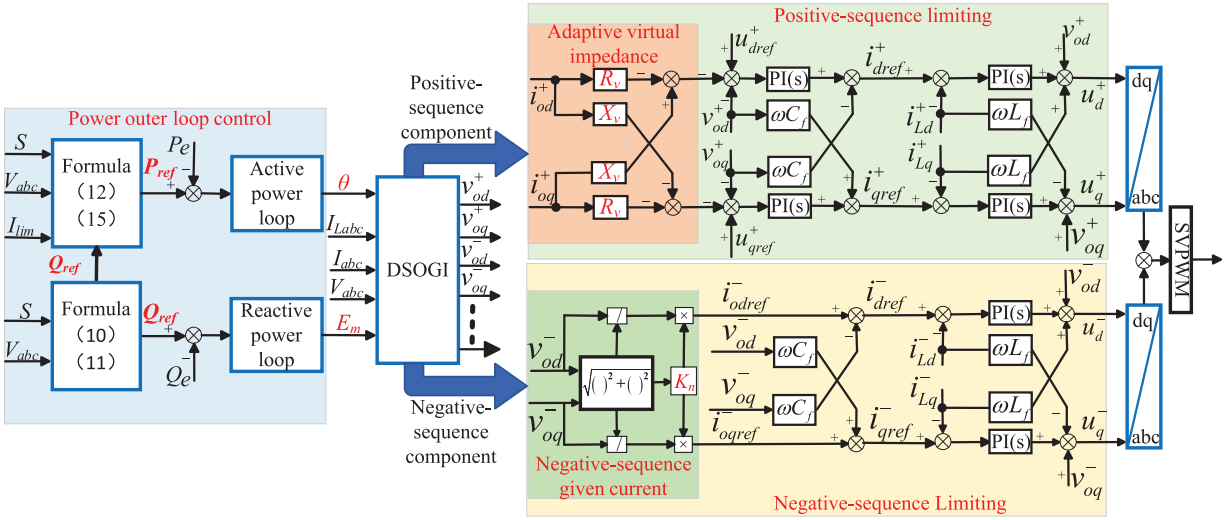

Figure 5: Coordinated inner and outer loop control structure for FRT

4.1 Dynamic Regulation of the Outer Power Loop

During grid voltage sags, the limited bandwidth of the power control loop causes sluggish reactive current adjustment. Concurrently, the excitation system fails to provide instantaneous voltage compensation,

resulting in insufficient reactive power. To address this, a dynamic reactive power compensation strategy is implemented to provide voltage support [28], as shown in Eqs. (12) and (13).

$$Q_{pu} = \begin{cases} 1.5 \times \left(U_{pu} - 1.1\right) \times S_{pu} & U_{pu} > 1.1 \\ 0 & 0.9 < U_{pu} \le 1.1 \\ 1.5 \times \left(0.9 - U_{pu}\right) \times S_{pu} & 0.2 < U_{pu} \le 0.9 \\ 1.05 \times S_{pu} & U_{pu} \le 0.2 \end{cases} \tag{12}$$

$$Q_{ref} = S \times Q_{pu} \tag{13}$$

where Q_{pu} represents the per-unit value of reactive power, U_{pu} denotes the per-unit value of the grid-side voltage amplitude, S_{pu} represents the per-unit value of apparent power, and S represents the apparent power.

To ensure smooth FRT and system stability, a coordinated control strategy encompassing active power control, δ limitation, and fault current suppression are required in addition to reactive power compensation. As analyzed in Section 2.1, the dynamic behavior of δ is crucial for transient stability during voltage sags. Maintaining δ within a bounded stability margin improves system stability. By constraining the active power reference, the acceleration area S_{acc} is reduced. According to the equal area criterion and the fault ride-through process shown in Fig. 3, the deceleration area also decreases accordingly, thereby shifting the fault power angle δ_g to the left. This ensures that $S_{acc} \le S_{dec}$, minimizing the deviation of δ, as illustrated in Fig. 6.

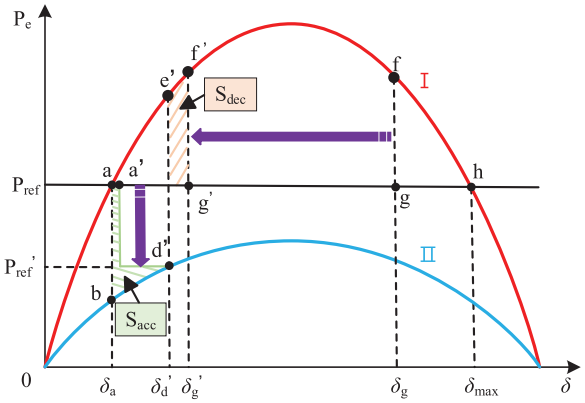

Figure 6: Improved active power loop's power angle curve

The capacity of grid-connected converters is limited by their rated apparent power capacity. During grid faults, active power is regulated according to the relationship with apparent power, and the specific control method is shown in Eq. (14).

$$P_{ref} = \min\left(\sqrt{S^2 - Q_{ref}^2}, P_{\lim}\right) \tag{14}$$

where P_{lim} represents the maximum limit amplitude of the active power reference value, determined by the fault current multiplier I_{lim}. Due to the influence of power electronic devices within converters, it is essential to prevent thermal breakdown, overcurrent shutdown, and reduced device lifespan during FRT events. Therefore, the control strategy should be designed in accordance with the IEEE 1547–2018 standard [27] for electric power systems, which is designed as 1.2 p.u. The per-unit amplitudes of the converter's active and reactive current components are denoted as $I_{pu,d}$ and $I_{pu,q}$, as shown in Eqs. (15) and (16), respectively.

$$I_{pu,q} = \frac{Q_{pu}}{U_{pu}} \tag{15}$$

$$I_{pu,d} = \sqrt{I_{pu,\lim}^2 - I_{pu,q}^2} \tag{16}$$

Thus, the maximum amplitude limit for obtaining the maximum active power reference value can be calculated using Eq. (17):

$$P_{\lim} = U_{pu} \times I_{pu,d} \times S \tag{17}$$

Through the dynamic regulation of active and reactive power, power angle deviation is minimized, the steady-state component of the fault current is reduced, and system stability is enhanced. At the same time, reactive power compensation is provided, offering strong voltage support on the grid side. However, the power control loop suffers from limitations such as narrow bandwidth and slow response, making it ineffective in controlling the transient components of the fault current during fault conditions. To address these transient issues, an analysis of the system's dynamic behavior is conducted, and virtual impedance is employed to achieve effective control.

4.2 Dynamic Regulation of Positive-Sequence Voltage and Current Loops

The narrow bandwidth and sluggish response of the power loop significantly impair its capability to regulate the transient fault current components. As derived from Eq. (11), adjusting the equivalent impedance can suppress the current amplification. Since R_f and L_f are fixed, an adaptive virtual impedance $Z_v = R_v + jX_v$, as illustrated in Fig. 7, is introduced prior to the outer voltage and current loops to limit the voltage reference value, thereby reducing the current reference value and effectively limiting the fault current [29]. The virtual impedance Z_v can be calculated by Eqs. (18) and (19).

$$R_V = \begin{cases} m(I_o - I_L) & if\ I_o \geq I_L \\ 0 & if\ I_o < I_L \end{cases} \tag{18}$$

$$X_V = n_{X/R} R_V \tag{19}$$

$$I_o = \sqrt{I_d^2 + I_q^2} \tag{20}$$

where m denotes the virtual impedance coefficient, $n_{X/R}$ represents the virtual impedance ratio, I_o is the root mean square (RMS) value of the fault current, while I_L is the fault current threshold. To enhance the robustness of overcurrent limitation, I_L is chosen to be slightly lower than I_{lim}, I_L = 1.1 p.u.

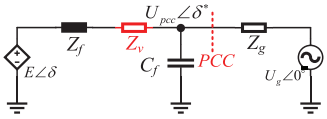

Figure 7: Equivalent circuit diagram with added Virtual Impedance

To accommodate various fault conditions, especially single-phase faults during voltage sags, the proposed control strategy dynamically adjusts the virtual impedance based on the maximum phase current. This aims to enhance the converter's FRT capability by limiting the fault current while preserving voltage source characteristics.

To quantify the current magnitudes, the phase currents are decomposed into positive-sequence and negative-sequence components. The dq-frame magnitudes are given by:

$$\begin{cases} I_P = \sqrt{\left(I_d^+\right)^2 + \left(I_q^+\right)^2} \\ I_N = \sqrt{\left(I_d^-\right)^2 + \left(I_q^-\right)^2} \end{cases} \tag{21}$$

Leveraging trigonometric functions, the current magnitudes in each phase (A, B, C) can be expressed as:

$$\begin{cases} I_A = \sqrt{I_P^2 + I_N^2 + 2I_P I_N \cos(\alpha)} \\ I_B = \sqrt{I_P^2 + I_N^2 + 2I_P I_N \cos(\alpha + 2\pi/3)} \\ I_C = \sqrt{I_P^2 + I_N^2 + 2I_P I_N \cos(\alpha - 2\pi/3)} \end{cases} \tag{22}$$

Here, the phase angle between the dq axes is denoted as $\varphi(\star)$, the composite phase angle difference α is defined as: $\alpha = \varphi(i_P) - \varphi(i_N) + \varphi(u_P) - \varphi(u_N)$. Therefore, the maximum effective value of the fault current can be expressed as:

$$I_{\max} = \max(I_A, I_B, I_C) \tag{23}$$

This value serves as a critical metric for limiting the peak fault current through virtual impedance control. To mitigate the instantaneous voltage drop caused by sudden current injection during the fault, a dynamic virtual impedance is applied. It is designed to generate a compensating voltage ΔU_m, defined as:

$$\Delta U_m = U_n \left(1 - U_{pu}\right) \tag{24}$$

$$U_{vx} = I_L \sqrt{R_v^2 + X_v^2} = I_o m \left(I_o - I_L\right) \sqrt{1 + n_{X/R}^2} \tag{25}$$

Based on Eqs. (23)–(25), the virtual impedance coefficient for the positive sequence component is derived as:

$$m = \frac{U_n \left(1 - U_{pu}\right)}{I_{\max} \left(I_{\max} - I_L\right) \sqrt{1 + n^2}} \tag{26}$$

By dynamically adjusting the virtual impedance coefficient, the virtual impedance can adapt to the severity of the fault current, thereby achieving effective current suppression and enhancing fault ride-through capability.

4.3 Negative Sequence Current Loop Control

Under unbalanced faults, controlling only the positive-sequence current exacerbates voltage distortion. Precise control of the negative-sequence current is required to enhance system stability. Due to the limitation of steady-state current, conventional power reference adjustment strategies become ineffective. To achieve balanced three-phase current output, the negative-sequence current reference is enforced to zero [30]. A feedforward decoupling algorithm is implemented, governed by the following dynamic equation:

$$\begin{cases} u_d^- = v_{od}^- + \left(K_p + \dfrac{K_I}{s}\right)\left(i_{dref}^- - i_d^-\right) + \omega L i_q^- \\ u_q^- = v_{oq}^- + \left(K_p + \dfrac{K_I}{s}\right)\left(i_{qref}^- - i_q^-\right) - \omega L i_d^- \end{cases} \tag{27}$$

Recent advancements in GFM converters research have introduced stringent requirements for negative-sequence current control. During asymmetrical faults, it is imperative to inject negative-sequence reactive power must be compensated to reduce negative-sequence voltage and improve power quality. Thus, a dedicated negative-sequence current loop is implemented to regulate the output current. The resultant negative- sequence active and reactive power can be expressed as:

$$\begin{cases} P^- = \left\|v^-\right\| \times i_{ac}^- = \sqrt{\left(v_{od}^-\right)^2 + \left(v_{oq}^-\right)^2} \times i_{ac}^- \\ Q^- = \left\|v^-\right\| \times i_{re}^- = \sqrt{\left(v_{od}^-\right)^2 + \left(v_{oq}^-\right)^2} \times i_{re}^- \end{cases} \tag{28}$$

where i_{ac}^- represents the negative-sequence active current, i_{re}^- represents the negative-sequence reactive current. In the dq coordinate system, the negative-sequence active and reactive powers can be further expressed as:

$$\begin{cases} P^- = v_{od}^- i_{od}^- + v_{oq}^- i_{oq}^- \\ Q^- = v_{od}^- i_{oq}^- - v_{oq}^- i_{od}^- \end{cases} \tag{29}$$

From Eqs. (28) and (29), it can be concluded that:

$$\begin{cases} i_{od}^{-} = \frac{v_{od}^{-}}{\sqrt{\left(v_{od}^{-}\right)^2+\left(v_{oq}^{-}\right)^2}} i_{ac}^{-} - \frac{v_{oq}^{-}}{\sqrt{\left(v_{od}^{-}\right)^2+\left(v_{oq}^{-}\right)^2}} i_{re}^{-} \\ i_{oq}^{-} = \frac{v_{oq}^{-}}{\sqrt{\left(v_{od}^{-}\right)^2+\left(v_{oq}^{-}\right)^2}} i_{ac}^{-} + \frac{v_{od}^{-}}{\sqrt{\left(v_{od}^{-}\right)^2+\left(v_{oq}^{-}\right)^2}} i_{re}^{-} \end{cases} \tag{30}$$

To inject negative-sequence reactive current into the inverter and offset the reverse voltage sags caused by the fault's negative-sequence voltage, i_{ac}^{-} is set to zero, i_{re}^{-} is set to a negative value, and the negative-sequence reactive current is linked to the voltage via a proportional coefficient K_n, $\|i_{re}^{-}\|$ represents the increment of the negative-sequence reactive current.

$$\| i_{re}^{-} \| = K_n \sqrt{\left(v_{od}^{-}\right)^2 + \left(v_{oq}^{-}\right)^2} \tag{31}$$

$$\begin{cases} i_{odref}^{-} = \frac{v_{oq}^{-}}{\sqrt{\left(v_{od}^{-}\right)^2+\left(v_{oq}^{-}\right)^2}} \| i_{re}^{-} \| \\ i_{oqref}^{-} = -\frac{v_{od}^{-}}{\sqrt{\left(v_{od}^{-}\right)^2+\left(v_{oq}^{-}\right)^2}} \| i_{re}^{-} \| \end{cases} \tag{32}$$

The reference values of the inverter's negative-sequence current are:

$$\begin{cases} i_{dref}^{-} = i_{odref}^{-} - \omega C_f v_{oq}^{-} \\ i_{qref}^{-} = i_{oqref}^{-} + \omega C_f v_{od}^{-} \end{cases} \tag{33}$$

5 Simulation Verification

The proposed control strategy aims to limit power imbalance, reduce δ fluctuations, and restrict fault currents to ensure equipment safety. In the FRT simulation, the voltage sag is applied on the grid side at the PCC, corresponding to U_{PCC}. The fault is initiated at t = 0.5 s and cleared at t = 1 s. To verify the effectiveness of the strategy, a converter model is built in MATLAB/Simulink, simulating symmetric and asymmetric faults. Some simulation parameters are shown in Table 1.

Table 1: System parameters design

Parameters	Value	Parameters	Value
DC voltage U_{dc}	750 V	AC rated voltage U_g	311 V/50 Hz
Filter inductors L_f	2 mh	Rated angular velocity ω_n	314 rad/s
Resistive R_f	0.1 Ω	Damping coefficient D_p	20 N·m·s/rad
Filter capacitors C_f	40 μF	Rotary inertia J	0.02 kg/m^2
Apparent power S	50 KV/A	Sagging coefficient D_q	0.01 N·m·s/rad
Scale factor K_n	0.2	Inertia control coefficient K	0.0001
Proportional gain K_{so}	1.2	Virtual impedance ratio $n_{X/R}$	5
Proportional gain k_{pu}	2	Proportional gain k_{pi}	10
Integral gain k_{iu}	100	Integral gain k_{iu}	500

5.1 Simulation Analysis of Symmetrical Faults

In the symmetrical FRT simulation, the fault occurs at t = 0.5 s, where the three-phase voltage sags from 1 to 0.2 p.u., and recovers to 1 p.u. at t = 1 s. The power regulation with fixed virtual impedance, which lacks

dynamic components, is taken as the baseline control strategy and compared with the improved coordinated inner- and outer-loop control strategy, as shown in Fig. 8. In the improved control simulation, the converter output is evaluated based on measurements at the PCC. The steady-state power angle of 0.126 radians during normal operation is selected as the base value and defined as 1 p.u. With this normalization, the active power output closely follows the reference, effectively mitigating power angle deviations during the fault period. A dynamic reactive power compensation loop is added to provide voltage support, while the adaptive virtual impedance suppresses the transient fault current, limiting it within 1.2 p.u., thereby ensuring system stability.

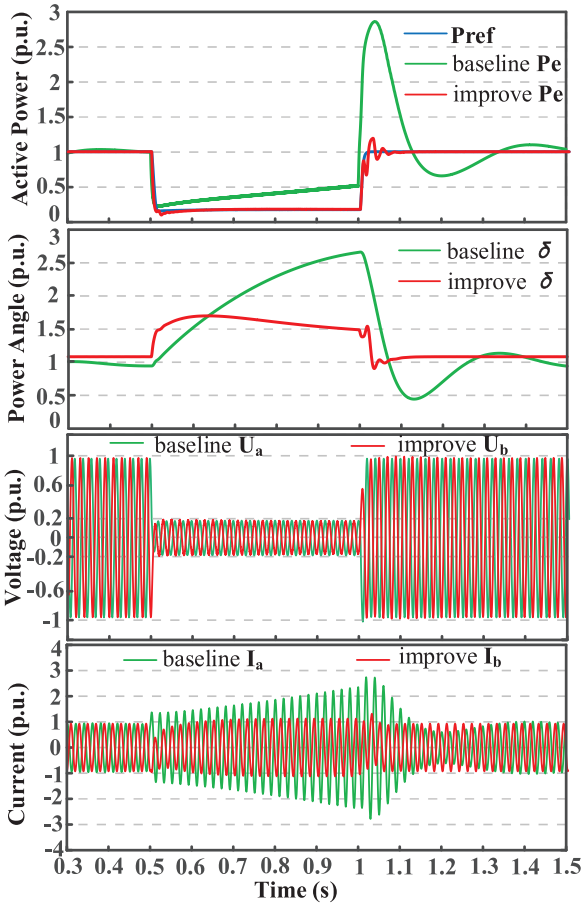

Figure 8: Performance comparison under symmetrical fault: improved vs. baseline control

5.2 Simulation Analysis of Asymmetrical Faults

In practical power grid operations, asymmetrical faults most commonly manifest as single-phase-to-ground faults and two-phase short-circuit faults. Therefore, to comprehensively evaluate the FRT capability of the proposed control strategy, this section conducts simulation analyses for both single-phase and two-phase fault scenarios, aiming to verify its adaptability and robustness under various types of asymmetrical faults. In the initial simulation analysis, a negative-sequence current suppression strategy is employed to ensure the inverter delivers balanced three-phase currents during fault conditions and to mitigate system impacts. Specifically, the control objective is set as $i_{dref}^{-} = i_{qref}^{-} = 0$, effectively suppressing the negative-sequence current to reduce system disturbances and prevent thermal damage to equipment. While this method demonstrates clear advantages in enhancing current output quality, it also presents certain limitations. Complete suppression of the negative-sequence current impairs the inverter's ability to

counteract negative-sequence voltage components from the grid, thereby restricting its capability to restore voltage symmetry. Consequently, Section 5.3 provides a separate analysis of a negative-sequence current compensation mechanism to address this issue.

Fig. 9 presents the simulation waveforms of active power, reactive power, power angle, output voltage, and output current under a single-phase-to-ground fault. The asymmetrical fault on the grid side is introduced at t = 0.5 s, where the voltage of phase A instantaneously drops from the rated value of 1.0 to 0.2 p.u., while the other two phases remain at the rated voltage. The fault is cleared at t = 1.0 s, and the grid voltage is restored to the rated level of 1.0 p.u. Fig. 10 shows the simulation results under a two-phase fault scenario. Similarly, the grid-side fault is applied at t = 0.5 s, during which the voltages of phases A and B drop from 1.0 to 0.2 p.u., while phase C remains unaffected. The fault is cleared at t = 1.0 s, and the system voltage returns to its nominal value of 1.0 p.u.

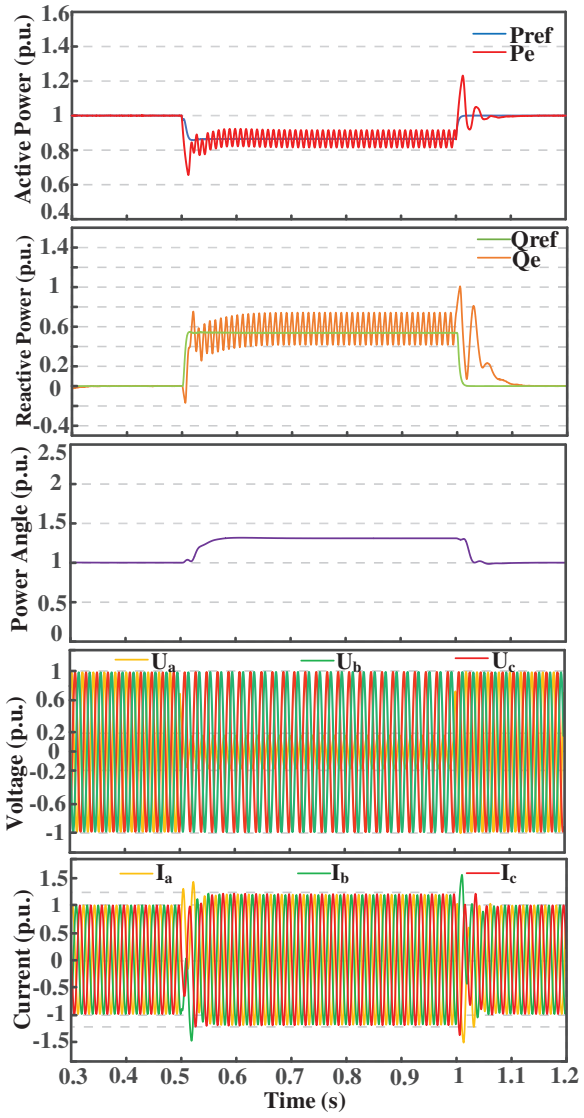

Figure 9: Waveform of single-phase ground fault

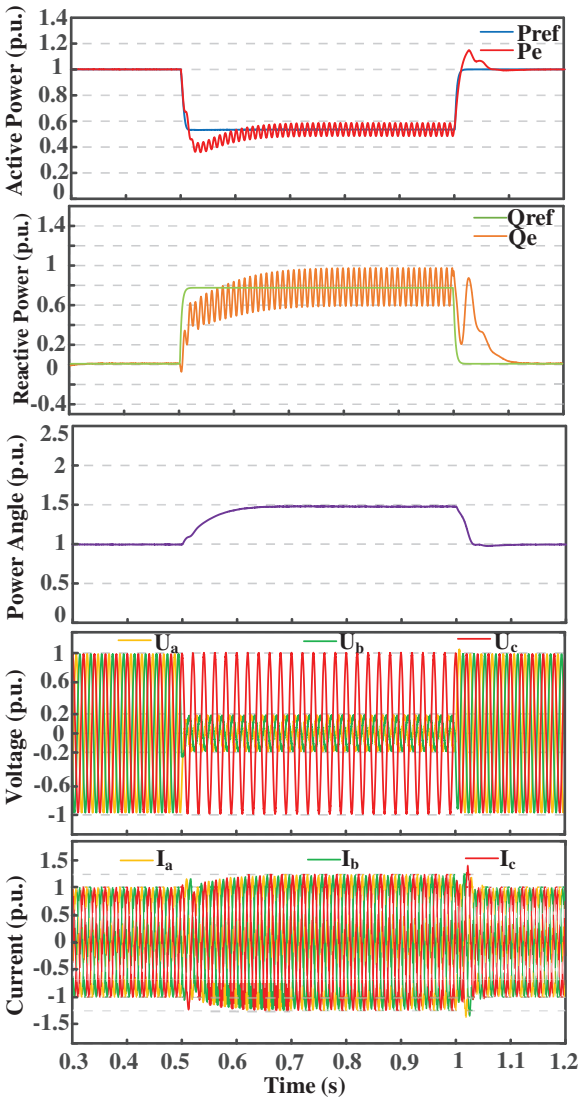

Figure 10: Waveform of two-phase short circuit fault

By utilizing a DSOGI, the fault voltages and currents are decomposed into positive- and negative-sequence components. While maintaining control over the positive-sequence components, the negative-sequence components are effectively suppressed. This approach mitigates double-frequency oscillations during the fault period, ensures that the active power P_e closely tracks the reference P_{ref}, limits the power deviation, and reduces power angle fluctuations. Meanwhile, voltage support is provided during the fault through reactive power compensation, and the fault current is constrained within the predefined threshold of 1.2 p.u.

5.3 Simulation Analysis of Negative-Sequence Reactive Current Compensation

Although the negative-sequence current suppression strategy discussed in Section 5.2 demonstrates significant advantages in terms of current output quality, it also presents certain limitations. Specifically, the complete suppression of the negative-sequence current renders the system incapable of effectively counteracting the negative-sequence voltage components from the grid, thereby limiting its ability to restore voltage

symmetry. To address this issue and effectively suppress the negative-sequence voltage generated during asymmetrical faults, a negative-sequence reactive current compensation mechanism described in Section 4.3 is introduced in the negative-sequence control loop. As shown in Fig. 11, when an asymmetrical fault occurs, the negative-sequence control loop outputs reactive current to compensate the grid, thereby mitigating the negative-sequence reactive voltage. Fig. 12 illustrates the waveform of the negative-sequence reactive voltage under both suppression and compensation strategies, highlighting the effectiveness of the compensation mechanism. It can be observed from the figure that, after introducing the negative-sequence reactive current compensation, a portion of the negative-sequence reactive voltage in the grid is offset. This results in a noticeable reduction of the negative-sequence reactive voltage, decreases voltage asymmetry on the grid side, and ultimately improves power quality.

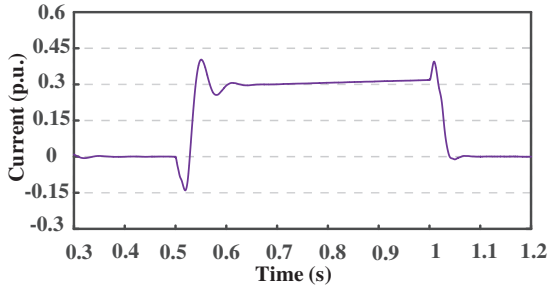

Figure 11: Negative-sequence reactive current compensation

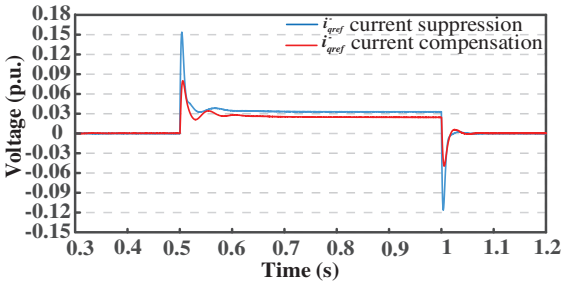

Figure 12: Negative-sequence voltage: suppression vs. compensation

To verify the performance of negative-sequence reactive current compensation under unbalanced fault conditions, a three-phase unbalanced fault scenario is configured. The fault occurs at t = 0.5 s, with A-phase voltage dropping to 0.2 p.u., B-phase to 0.4 p.u., and C-phase to 0.6 p.u., with fault clearance at t = 1 s and grid voltage recovering to 1 p.u. In Fig. 13, to ensure balanced three-phase current output and reduce system impact, a negative-sequence current suppression strategy was used, setting $i_{dref}^{-} = i_{qref}^{-} = 0$ to reduce disturbance and prevent thermal damage to the equipment. By controlling the positive-sequence components and suppressing the negative-sequence components, the double-frequency oscillations during the fault are reduced. Simultaneously, the active power P_e closely follows the reference P_{ref}, limiting power deviations and minimizing δ fluctuations, with the fault current constrained within 1.2 p.u.

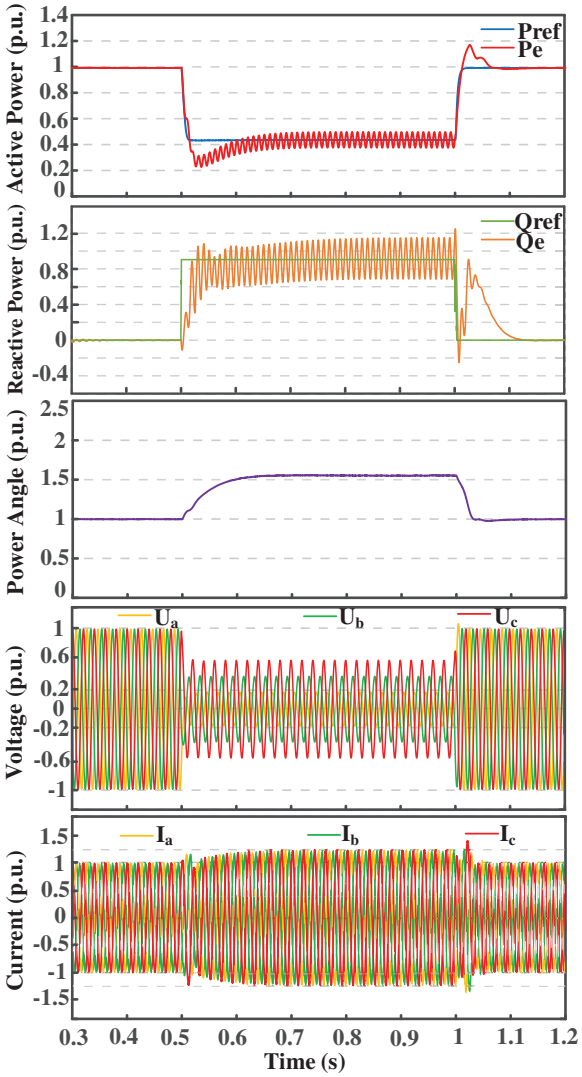

Figure 13: Simulation waveforms under negative-sequence reactive current suppression

Fig. 14 presents the simulation waveforms of asymmetrical fault conditions with negative-sequence reactive current compensation. Although the fault current slightly increases after introducing negative-sequence reactive current compensation compared to Fig. 13 without compensation, and an imbalance in the three-phase output currents appears, this is due to the injection of negative-sequence reactive current. This injection is equivalent to the inverter actively outputting a set of asymmetric current components superimposed on the original symmetrical positive-sequence current components. This is a deliberate trade-off by the inverter to compensate for grid imbalance and support the voltage.

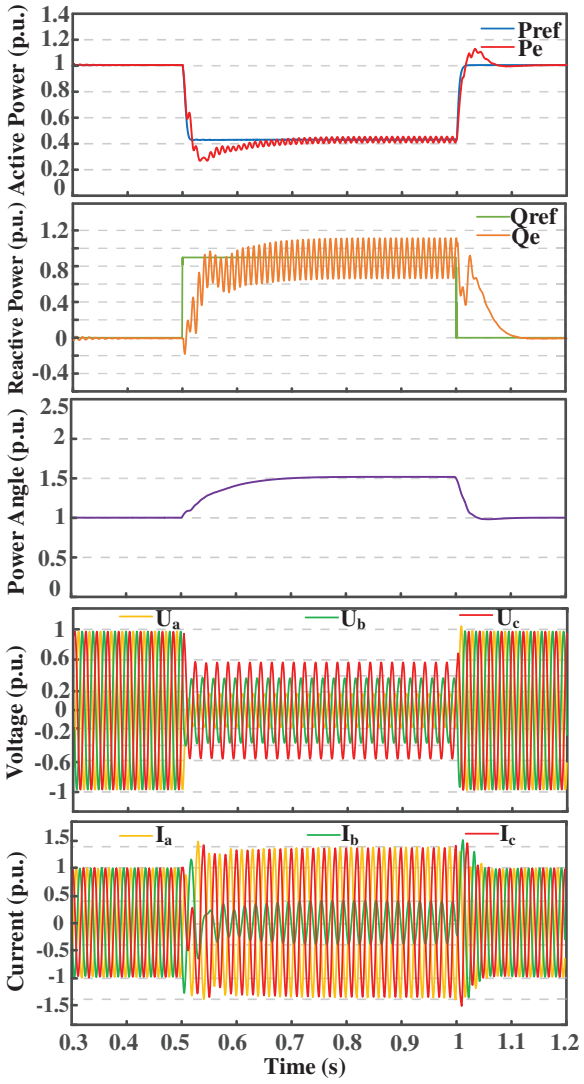

Figure 14: Simulation waveforms under negative-sequence reactive current compensation

6 Conclusion

In the context of fault ride-through for GFM converters, the proposed control strategy enables ride-through under various fault types, while maintaining voltage source characteristics, and providing effective voltage support. Key conclusions are as follows:

(1) An improved control strategy based on dynamic adjustment of the reference power is proposed for the outer power loop, effectively mitigating power angle deviation caused by active power imbalance. At the same time, adaptive reactive power compensation is performed according to the severity of the voltage sag, providing effective voltage support for the grid. This control strategy significantly enhances the system's dynamic response and robustness.

(2) An adaptive virtual impedance is introduced to optimize the inner current control loop. By appropriately designing the virtual impedance parameters, effective limitation of fault currents under various fault types and severities is achieved. This enhances the system's adaptability under fault conditions and ensures safe and stable operation.

(3) To address unbalanced faults, the introduced negative-sequence reactive current compensation effectively reduces the negative-sequence voltage components, significantly improving the voltage imbalance of the power grid. This enhances the voltage symmetry of the power system and improves overall power quality. Meanwhile, the proposed compensation strategy strengthens the system's dynamic response and operational stability, providing a solid foundation for the secure and reliable operation of the grid.

Future work will focus on enhancing the engineering applicability and deployment scope of the proposed multi-loop coordinated control strategy. Hardware-in-the-loop (HIL) simulations and experiments will be conducted to verify its effectiveness and robustness under practical conditions. The strategy will also be extended to coordinated control of multiple GFM converters, high-penetration renewable systems, and AC/DC hybrid microgrids, with further investigation into its performance under communication delays and system disturbances.

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Availability of Data and Materials: The authors confirm that the data used in this study are available on request.

Ethics Approval: Not applicable.

Conflicts of Interest: The authors declare no conflicts of interest to report regarding the present study.

Abbreviations

GFM	Grid-Forming
FRT	Fault ride-through
GFL	Grid-Following
RES	Renewable energy sources
DSOGI	Dual second-order generalized integrator
VSG	Virtual synchronous generator
SGs	Synchronous generators

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