Computers, Materials & Continua

Tech Science Press

https://doi.org/10.32604/cmc.2026.080058

ARTICLE

Low-Noise, High-Gain 28 GHz LNA Design Using Multi-Objective Optimization with NSGA-II and MOPSO

Spandana Saggurthi[1], Anand Nayyar[2], Sk Hasane Ahammad[1] and Sumendra Yogarayan[3,*]

[1]Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation, Andhra Pradesh, India
[2]School of Computer Science and Artificial Intelligence (SCA), Duy Tan University, Da Nang, Vietnam
[3]Faculty of Information Science and Technology, Multimedia University, Melaka, Malaysia

*Corresponding Author: Sumendra Yogarayan. Email: sumendra@mmu.edu.my

Received: 02 February 2026; Accepted: 02 April 2026; Published: 23 July 2026

ABSTRACT: This work presents a multi-objective optimization framework for systematic design-space exploration of a 28 GHz single-stage cascode LNA (Low noise amplifier) in 22 nm FDSOI technology using NSGA-II and MOPSO algorithms. The objectives of the paper include simultaneous minimization of noise figure (NF) and power consumption while maximizing gain under matching and stability constraints. Using device parameters and circuit models that were developed for a 22 nm FDSOI process technology, an optimization framework was created in Python, with the passive components L_G, L_S, L_D, L_{OUT}, and C_{OUT} chosen to be the variables optimized. The NSGA-II optimized design achieves 1.7 dB NF, 17 dB gain, and 4.7 mW DC power, while MOPSO achieves 1.8 dB NF, 17.1 dB gain, and 5.0 mW power. NSGA-II provides improved Pareto diversity and slightly better output matching, whereas MOPSO reduces computational time by 24% with comparable RF performance. The results demonstrate effective multi-objective design-space exploration and controlled algorithm benchmarking at the schematic-level for mm-wave LNA design.

KEYWORDS: LNA; mm-wave; multi-objective optimization; NSGA-II; MOPSO; internet of things (IoT); S-parameters; gain and noise figure

1 Introduction

The recent development of mm-wave technology for IoT has provided new possibilities in wireless communication [1] by introducing higher data rates, less latency, and increased network capacity. The 28 GHz frequency band is specifically of great interest for potential future IoT networks due to its good propagation characteristics and available bandwidth. But creating radio frequency (RF) front-end elements for such higher frequencies is a significant challenge, particularly for LNAs that are the key first active stage in receiver [2] chains. LNAs at mm-wave frequencies need to meet several conflicting performance requirements at the same time. The amplifier needs to have enough gain to amplify weak received signals while adding as little noise as possible, all with reasonable power consumption for energy-limited IoT devices. The mm-Wave design is particularly challenging at 28 GHz because of increased parasitics, lower transistor gain, and greater sensitivity to layout tolerance. Designers rely on their intuition and manually adjust parameters in traditional LNA design techniques that do not allow designers to fully explore the potential of all of the possible design options as such, they are often forced into making less than optimal trade-off decisions when it comes to the performance metrics of an LNA design. Traditional methods typically address

one aspect of performance at a time (e.g., gain or NF) using iterative simulation methods that can be slow and cumbersome to use for high-frequency designs.

The emergence of computational intelligence methodologies provides promising substitutes to address these drawbacks. Evolutionary and swarm intelligence methods, specifically, have shown tremendous potential in addressing difficult multi-objective optimization issues in many areas of engineering. The methods have the ability to traverse large design spaces with minimal effort, manage competing objectives, and identify non-obvious solutions that may not be apparent to humans. Among the most efficient computational intelligence methodologies, the non-dominated sorting genetic algorithm II (NSGA-II) and multi-objective particle swarm optimization (MOPSO) are notable for their efficacy in multi-objective optimization problems. NSGA-II utilizes the natural selection and genetic variation principles to evolve a population of solutions to optimal trade-offs. NSGA-II implements mechanisms of non-dominated sorting and crowding distance to preserve diversity and determine pareto-optimal solutions. MOPSO imitates the flocking of birds or schooling of fish, in which particles navigate in the solution space based on their own history and that of neighboring particles. Even though the use of these computational intelligence methods holds great promise, their extension to mm-Wave LNA design is not extensively explored, especially for IoT scenarios where power budgets are particularly limited. Optimizing key LNA characteristics of gain, noise factor, and total power dissipated in a single system represents an unprecedented multi-objective problem requiring a thoughtfully constructed problem definition and the tuning of algorithmic components.

There have been numerous investigations conducted on the utilization of evolutionary algorithms and swarm intelligence algorithms for optimizing RF circuits. Studies such as Ghosh et al. (2020) [3] utilized Moth–Flame Optimization to create a low-power LNA, where as Andrew Roobert et al. (2019) [4] implemented Elephant Herding Optimization techniques to create noise cancellation LNAs. Many other metaheuristic algorithms such as Genetic Algorithm, Firefly Algorithm, Flower Pollination Algorithm, and Cuckoo Search have also been studied for optimizing LNA and Analog circuit designs using algorithms [5–10]. There are other studies utilizing analytical methods that integrate evolutionary algorithms with device models. Several of these studies focus on optimizing one performance metric or fixed design specifications as such, they do not provide for systematic evaluation of design tradeoffs between multiple RF performance parameters, therefore, providing less opportunity for designers to choose operating characteristics necessary to meet application requirements.

Overall, earlier research has shown that evolutionary and swarm optimization algorithms are applicable to RF circuit design. However, variations in the operational frequency, technology node, objective definition and constraint handling make direct performance comparisons across studies difficult. This variability supports the need for controlled evaluation framework(s) that provides fair benchmarking and easy-to-understand exploration of design space.

Previous works on RF optimization using NSGA-II and MOPSO provide little insight into the application of multiple algorithms for the design of a 28 GHz Low Noise Amplifier (LNA) in an advanced 22 nm technology node [11]. The existing literature only covers individual algorithm implementations or discrete technology processes. This work provides new quantitative benchmarking for both NSGA II and MOPSO applied specifically to LNA designs at 28 GHz, utilizing tools that will allow for a complete exploration of the design space as well as a quantitative analysis of RF-to-computational tradeoffs. The objective of the research is to determine whether either NSGA-II or MOPSO is suited for optimizing a 28 GHz cascode LNA with inductive degeneration fabricated in 22 nm technology using the same algorithms and simulations under the same restrictions. The work employs a complete integration of circuit simulation tools and optimization algorithms into an end-to-end (E2E) optimization framework, facilitating thorough exploration of complex

design spaces through the concurrent optimization of the three most critical performance metrics (gain, noise figure, power consumption).

The objectives of the work are:

1. Systematic dual-algorithm benchmarking of NSGA-II and MOPSO for 28 GHz LNA optimization in 22 nm FDSOI technology, enabling controlled comparison under identical computational budgets and constraint handling.
2. Pareto trade-offs between noise figure, gain, and power consumption while meeting matching and stability constraints are revealed by explicit multi-objective design-space exploration.
3. Quantitative RF-performance vs. computational-cost trade-off analysis, showing sub-2 dB NF (1.7 dB) performance and demonstrating that while MOPSO reduces runtime by 24% with comparable RF performance, NSGA-II improves diversity and output matching.

These contributions collectively highlight the novelty and impact of this work in extending evolutionary multi-objective optimization to the design of high-performance, low-power mm-wave LNAs for future IoT front-end systems.

Organisation of the paper:

The rest of the paper is organized as: Section 2 presents the LNA circuit topology and design considerations. Section 3 formulates the multi-objective optimization problem. Section 3 details the implementation of NSGA-II and MOPSO algorithms. Section 4 presents the experimental results and comparative analysis. Finally, Section 5 concludes the paper.

2 LNA Circuit Topology and Design Considerations

2.1 Single-Stage Cascode Topology

The mm-wave LNA architecture employs a one-stage cascode topology with inductive degeneration, as presented in Fig. 1 The structure consists of a common-source (CS) stage and a cascaded common-gate (CG) stage to realize a good amplifier structure widely used in RF circuit design due to its excellent performance characteristics at high frequencies. The lower CS transistor M_{1CS} is the main amplifying device and is biased to the best current density for minimum noise figure with a suitable level of transconductance for gain. M_{1CS} employs multiple fingers to minimize gate resistance and maximize noise performance. The M_{1CG} top CG transistor is sized and biased appropriately to generate adequate isolation and reduce the Miller effect, while its body can be forward biased to improve linearity and reduce supply voltage performance. The input stage [12] is a source inductor (L_S) and gate inductor (L_G) that together transform the 50ohm source impedance to achieve the best noise and power matching conditions. The source inductor (L_S) also provides local feedback, which improves linearity and stability. Between the CS and CG modes, there is a coupling capacitor C_1 providing DC isolation as well as RF signal coupling, whose value can be designed to control the RF voltage swing on the gate of the cascode device.

The output section comprises a drain inductor (L_D) and output coupling capacitor (C_{OUT}) that form the output matching network. This network transforms the high output impedance of the cascode stage to match the 50ohm load impedance required for maximum power transfer.

The gain of the single-stage cascode LNA can be expressed in Eq. (1).

$$\text{Gain} = \left\{\frac{Z_{\text{in}}}{Z_{\text{in}} + R_s}\right\} \times \frac{gm_1 \times gm_2 \times R_{\text{out}}}{gm_2 + 1/r_{bib4}} \times \left(\frac{Z_L}{Z_L + R_{\text{out}}}\right) \tag{1}$$

where:

$$Z_{\text{in}} = sL_s + \frac{1}{sC_{gs}} + gm_1L_s + sL_g \tag{2}$$

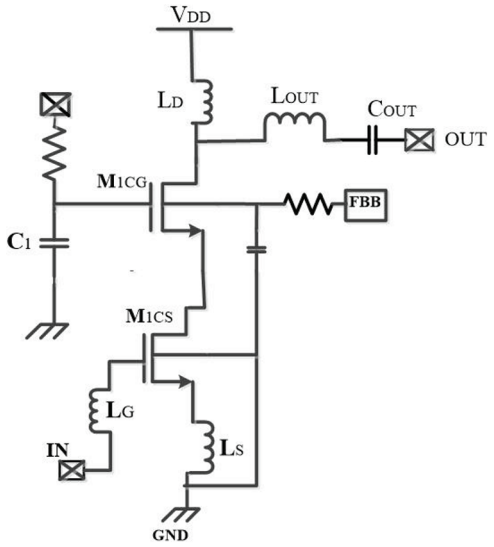

Figure 1: Single-stage cascode LNA.

Z_{in} is the input impedance as shown in Eq. (2), comprising the source inductor (L_s), gate-source capacitance (C_{gs}), transconductance of the input transistor (gm_1), and the gate inductor (L_g).

Z_L is the load impedance, which is a parallel combination of drain inductance (L_d), output capacitance (C_{out}), and output resistance (R_{out}), where each component's impedance contributes to the overall load impedance.

$$R_{\text{out}} = gm_2 \times r_{o1} \times r_{o2} \tag{3}$$

R_{out} is the output resistance of the cascode stage as shown in Eq. (3), where r_{bib3} and r_{bib4} are the output resistances of the M_{1cs} and M_{1cg} transistors, respectively.

The noise figure of the circuit can be expressed as a function of the minimum noise figure (NF_{min}), source admittance (Y_s), and optimal admittance (Y_{opt}). The complete expression is given in Eq. (4).

$$NF = NF_{\text{min}} + \frac{4R_s|Y_s - Y_{\text{opt}}|^2}{(1 + Y_{\text{opt}}R_s)^2} \tag{4}$$

where R_s represents the source resistance. The minimum noise figure (NF_{min}) is characterized as shown in Eq. (5).

$$NF_{\text{min}} = 1 + k\sqrt{gm(R_G + R_s)}\left(\frac{f}{f_T}\right) \tag{5}$$

with f_T as shown in Eq. (6) being the unity gain frequency, defined as:

$$f_T = \frac{gm_1}{2\pi C_{gs}} \tag{6}$$

The admittance parameters are defined through their relationships with impedance, where the source admittance Y_s is the inverse of the input impedance as shown in Eq. (7).

$$Y_s = \frac{1}{Z_{\text{in}}} \tag{7}$$

and the optimal admittance Y_{opt} as shown in Eq. (8) is the inverse of the optimal impedance.

$$Y_{\text{opt}} = \frac{1}{Z_{\text{opt}}} \tag{8}$$

The optimal impedance Z_{opt} as shown in Eq. (9) is further defined by the complex expression.

$$Z_{\text{opt}} = \frac{1}{gm} + j\left(\frac{1}{2\pi f C_{gs}} - 2\pi f L_s\right) \tag{9}$$

where gm represents the transconductance, C_{gs} the gate-source capacitance, and L_s the source inductance.

All inductors were modeled as on-chip spiral inductors using the foundry-provided, EM-based component models available in the 22 nm FDSOI. These models include frequency-dependent resistance, substrate losses, and coupling effects up to 40 GHz, providing realistic inductor behavior for schematic-level simulation. The output coupling capacitor and all bias decoupling capacitors were modeled as MIM (metal–insulator–metal) capacitors with a quality factor greater than 50. The input and output matching networks were designed using lumped LC elements rather than transmission lines to achieve compact integration. All devices and passive components included PDK-provided RC and EM parasitic models to ensure realistic simulation accuracy.

Table 1 detailed design information, all devices and biasing parameters were defined using 22 nm FDSOI PDK models. The common-source transistor (M_{1CS}) has a total width of 20 μm (10 fingers × 2 μm each) and a channel length of 22 nm. It is biased at a drain current of 2.8 mA, gate–source voltage of 0.75 V, and drain–source voltage of 0.85 V. The cascode transistor (M_{1CG}) has a total width of 16 μm (8 fingers × 2 μm each) and gate–source voltage of of 0.65 V. Both transistors use a +0.5 V forward body bias to enhance transconductance and linearity by utilizing the FDSOI back-gate feature.

Table 1: Transistor and passive component parameters.

Parameter	Value/Setting
Technology	22 nm FDSOI CMOS
M_{1CS}	Width = 20 μm (10 × 2 μm), Length = 22 nm
M_{1CG}	Width = 16 μm (8 × 2 μm), Length = 22 nm
Total drain current	2.8 mA
Supply voltage (V_{DD})	1.6 V
Gate–source voltages ($V_{GS,CS}/V_{GS,CG}$)	0.75 V/0.65 V
Drain–source voltage ($V_{DS,CS}$)	0.85 V
Body bias	+0.5 V (forward)
$L_G/L_S/L_D/L_{OUT}$	550/120/300/60 pH (modeled as spiral inductors)
C_{OUT}	100 fF (modeled as MIM capacitor)
Q-factor @ 28 GHz	15–22 (spirals), >50 (MIM)
Matching network	Lumped LC network (on-chip modeled)

2.2 Design Considerations for 28 GHz Operation

The design of an LNA for 28 GHz operation in 22 nm FDSOI technology creates numerous application-specific obstacles that can affect both component selection and optimization. Component Sizing is a primary concern since parasitic affects have a significant impact on LNA performance at such high frequencies and the size of transistor M_{1CS} has a direct relationship with its three most important parameters of noise figure, gain, and power consumption whereas, the size of transistor M_{1CG} has a direct relationship with its two most important parameters of isolation and gain. Inductive degeneration via the source inductance L_S performs two functions of impedance matching and improving linearity and requires a careful consideration of all three aspects of noise matching, input matching, and stability in order to optimize the LNA. Input and output Matching Networks must be designed so as to match the impedance of the LNA to the external environment at 28 GHz frequency, where parasitic effects and transmission line behavior become a dominant force. Constraints on Power Consumption are a major issue in IoT applications, which limits the bias current flowing through the cascode stack and directly affects the gain and noise performance of the LNA.

The 22 nm FDSOI Technology offers advantages including reduced parasitic capacitance and improved high-frequency performance compared to bulk CMOS, though it introduces unique considerations for body biasing and substrate coupling that must be accounted for in the design process. The most critical performance parameters of the 28 GHz LNA optimization are Gain (S_{bib32}), which is the gain of forward transmission aimed to be optimized for proper signal amplification. Noise Figure, a measure of signal-to-noise ratio degradation introduced by the LNA, aimed to be minimized. power consumption, power drawn by the LNA, which is especially important in IoT applications and aimed to be minimized. Input return loss (S_{bib22}), a measure of input impedance matching quality, aiming to be less than −10 dB and Output Return Loss (S_{bib33}), a measure of output impedance matching quality aiming to be less than −10 dB. Reverse isolation (S_{bib23}), output-to-input transmission, aiming to be minimized to avoid oscillations and stability factor (K), ensuring that the LNA is stable under all operational conditions, with a target of $K > 1$.

Although body biasing was not actively varied in the optimization loop, the design employs fixed forward biases of +0.3 V M_{1CS} and +0.2 V M_{1CG} to exploit FDSOI's back-gate control for improved transconductance and noise performance. Prior studies in 22 nm FDSOI LNAs indicate that such biasing can reduce NF by up to 0.2–0.3 dB and improve gain by approximately 0.5 dB at 28 GHz.

3 Multi-Objective Optimization

Multi-objective optimization [13–15] is applied to problems that have more than one competing goal for which there does not exist a single optimal solution that maximizes all the criteria simultaneously. Instead of one optimal solution, it obtains a set of Pareto-optimal solutions which are the optimal trade-offs between objectives. It is especially useful in RF circuit design, where inherently conflicting with one another are performance specifications such as gain, noise figure, and power consumption. Multi-objective optimization techniques give designers a number of optimal solutions from which they can select according to specific application requirements.

3.1 Design Variables and Objective Functions

The optimization of the 28 GHz LNA [16] requires the careful selection of key design variables that significantly impact performance metrics. These variables include passive component values (L_G, L_S, L_D, L_{OUT}, C_{OUT}). Based on the critical performance metrics, we formulate three primary objective functions.

1. **Minimize Noise Figure:** $f_1(X) = NF(X)$
2. **Maximize Power Gain:** $f_2(X) = -S_{bib32}(X)$
3. **Minimize Power Consumption:** $f_3(X) = P_{DC}(X) = V_{DD}(X) \cdot I_{DC}(X)$

Here, S_{21} denotes the simulated forward gain in decibel (dB) scale. These objectives are subject to the following constraints:

- Input/output matching: $S_{11}, S_{22} \leq -10$ dB
- Reverse isolation: $S_{12} \leq -20$ dB
- Stability: $K > 1$
- Minimum gain: $S_{21} \geq 15$ dB
- Minimum noise figure: NF < 2 dB
- Operation frequency: 28 GHz

To ensure that all feasible solutions satisfy the required RF performance specifications, a penalty-based constraint handling approach was employed during the fitness evaluation of both NSGA-II and MOPSO algorithms. To account for constraint violations in each objective function, a penalty function has been added, which adds a penalty to the objective value depending on how much worse a candidate solution violates a condition. The penalty function is a proportion of the square of the normalized amount of the constraint violation. This ensures that infeasible solutions are automatically ranked lower or dominated by feasible ones in the optimization process. The penalty weight was empirically set to a sufficiently high value ($\beta = 1000$) to prevent premature convergence toward non-physical or unstable designs. This formulation allows the evolutionary algorithms to explore the design space efficiently while maintaining compliance with RF design constraints.

3.2 Design Parameters and Optimization Range

The performance of the LNA has been optimized by evaluating various parameters shown in Table 2 of critical passive components. These include gate inductance (L_G), which ranges from 500 to 600 pH, in order to achieve maximum resonance and appropriate impedance matching at the operating frequency. Of the different parameters considered during testing, source inductance (L_S), which was tested within a range of 100 to 200 pH and drain inductance (L_D), tested within a range of 200 to 350 pH, had the greatest effect on noise figure and gain. An output inductance (L_{OUT}) ranging from 40 to 80 pH was used in order to ensure optimal load matching of the LNA. Likewise, an output capacitance (C_{OUT}) range from 80 to 120 fF was used in order to assist with bandwidth tuning and maintain overall circuit stability. These parameter ranges were derived from realistic device models, and historical design guidelines were employed as the search space for the optimization algorithms applied. Defining the bounds of the search space ensures that the LNA designs produced will have both physical viability and performance competitiveness.

Table 2: Optimization variables and search ranges.

Parameter	Description	Range
L_G	Gate inductance	500–600 pH
L_S	Source inductance	100–200 pH
L_D	Drain inductance	200–350 pH
L_{OUT}	Output inductance	40–80 pH
C_{OUT}	Output capacitance	80–120 fF

3.3 NSGA-II Algorithm

NSGA-II is an evolutionary algorithm illustrated in Fig. 2 that has special characteristics for multi-objective optimization. Specifically, Pareto dominance and elitism both help to maintain diversity in the

population of the individuals within the allowed set solutions to keep viable solutions thus providing improved performance.

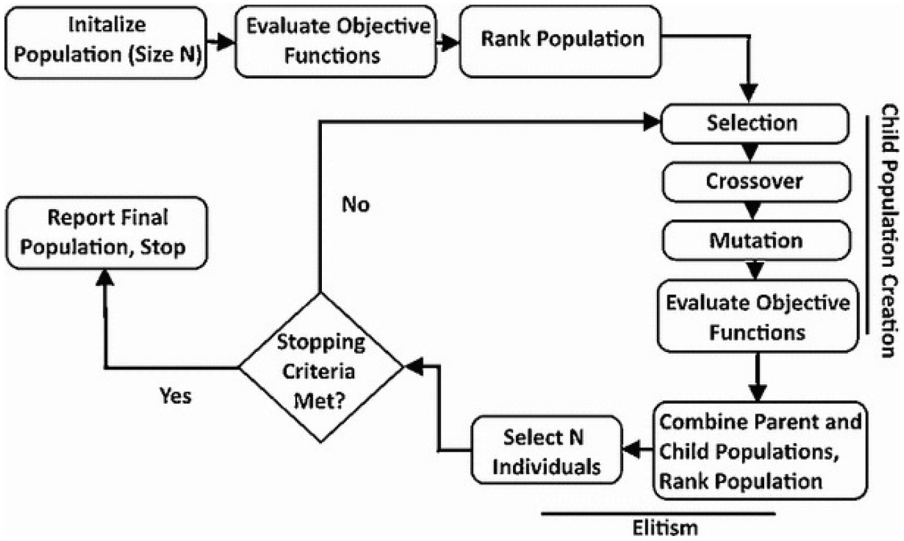

Figure 2: Flow chart of NSGA-II.

The Non-dominated Sorting Genetic Algorithm II (NSGA-II) is a multi-objective [17] evolutionary optimization [18,19] technique that begins with the generation of an initial population sampled randomly from the design variable constraints. Solutions for the different design variables are evaluated by running a model of the design on a circuit simulator and determining values for multiple objectives, such as noise figure, gain, and power consumption. Models evaluated by simulation are then assigned to a Pareto front using the concept of non-domination classification. The algorithm implements solution diversity using a crowding distance metric that measures relative separation between solutions within each Pareto front. Parent solutions are selected using binary tournament selection techniques, with preference given to the lowest [20] ranked non-dominated front solutions and the highest crowding distance measure solutions. Genetic Operators like Simulated Binary Crossover (SBX) and polynomial mutation create offspring from parents through adding controlled variation. The parents and the offspring populations are combined and sorted after recombination, and only the fittest of these populations will reproduce into the next generation. This process of recombination and subsequent reproduction into the next generation continues for a specific number of generations or until an acceptable degree of convergence has been reached. The two primary contributions of NSGA-II relate to an elitist method of retaining the best individuals of any population and a method of using crowding distances to prevent individuals from clustering [21] to maintain appropriate computational complexity of $O(MN^2)$ without eliminating [22] the need for fixed sharing parameters.

3.4 Multi-Objective Particle Swarm Optimization

Particle Swarm Optimization [23] is a stochastic optimization approach where particles move in a way that exhibits social behaviour similar to that of birds or fish [24]. This algorithm allows for searching through complex spaces of possible designs by having the particles move together in coordination. Each particle will update its trajectory depending upon its experience as well as those of its neighbours. This work uses a Multi-Objective PSO (MOPSO) [25] which extends the normal PSO by adding an external archive of non-dominated solutions and employing a leader selection mechanism for achieving Pareto dominance against crowding distance to maintain diversity Fig. 3. Each particle's fitness is determined from circuit-level

simulations and the particles move together iteratively towards the Pareto optimal front indicating tradeoffs in terms of gain, noise figure, and power consumption.

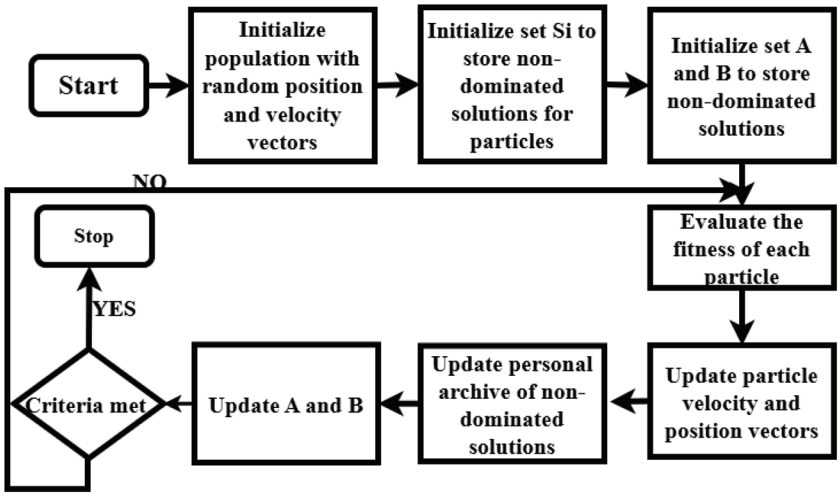

Figure 3: Flow chart of MOPSO.

The velocity of a particle [26] as it travels along a path is updated based on its inertia weight, cognitive and social learning and includes a stochastic component to encourage exploration of the space being searched. As particles move through the design space, modifications to their location keep them within the plausible domain through the use of boundary handling techniques. The multi-objective approach to particle swarm optimization (PSO) has introduced an external archive that evolves continually with the addition of non-dominated solutions and the deletion of dominated solutions using the archive from the archive as new non-dominated solutions. Using this technique, MOPSO has successfully approximated the Pareto front with a range of diverse solutions while being able to address LNA optimization through tailored initial conditions based on experience with low noise amplifier designs, by applying penalty functions as constraint enforcement mechanisms, and using parallel circuit simulations to estimate performance metrics. MOPSO is an effective method for finding good solutions to LNA design problems as it has many advantages, including: easy implementation, high-speed convergence [27], ability to efficiently perform global searches, low memory requirements, and no dependence on derivatives.

3.5 Algorithm Configuration

The assessment of the performance of each algorithm was based on their most recent implementation versions at the time, with both algorithms being assigned the same computational limitation of 10,000 function evaluations. The main configuration parameters used for the NSGA-II and MOPSO algorithms, including population size, iteration count, crossover and mutation probabilities, and swarm coefficients, are summarized in Table 3. The selected empirical penalty factor for both algorithms ($\beta = 1000$) was predicted to sufficiently distance infeasible solution from feasible solutions by creating a smaller separation between objective scaling and infeasibility penalty. The initial tests on β-values of 500–2000 demonstrated that minimal fluctuations in the penalty factor produces no noticeable changes to the shape of the generated pareto fronts and their overall performance metrics (change < 2%–3%). The value chosen allows for consistent convergence with clear delineation between feasible and infeasible regions within the design space created using latin hypercube sampling to create an evenly distributed initial population across the design space. Constraint violations ($S_{11} > -10$ dB, $S_{22} > -10$ dB, $S_{21} > -20$ dB, $K < 1$, $S_{21} < 15$ dB, NF > 2 dB) were

treated with a penalty based method and resulted in lower fitness for infeasible solutions proportionate to their degree of infeasibility. Each algorithm ran 10 independent times with different random seeds the results of each run were compiled and the median of each used for comparisons.

Table 3: Algorithmic parameters.

Parameter	NSGA-II	MOPSO
Population/Swarm Size	100	100
Iterations	100	100
Total Evaluations	10,000	10,000
Crossover Probability (pc)	0.9	–
Mutation Probability (pm)	0.1	–
Crossover Type	SBX (nc = 20)	–
Mutation Type	Polynomial (nm = 20)	–
Selection	Binary tournament	–
Inertia Weight (w)	–	0.9 → 0.4
Cognitive Coeff. (c1)	–	2.0
Social Coeff. (c2)	–	2.0
Archive Size	–	50
Constraint Penalty (β)	1000	1000
Statistical Runs	10	10

To assess how robust the obtained findings are, a brief sensitivity analysis was performed, varying select algorithm parameters while ensuring all the remaining settings are held constant. For example, for NSGA-II, both the population size (80 to 120 individuals) and mutation probability (0.05 to 0.15) were varied. For MOPSO, the inertia weight (0.3 to 0.8) and (0.5 to 1.0) among but the cognitive number and social numbers remained the same. The resulting Pareto fronts and final performance metrics (NF, S_{bib32}, and power) showed only minor variations (<3% change in objective values), and the relative comparison between NSGA-II and MOPSO remained consistent. This suggests that the conclusions regarding convergence performance and diversity are not extremely sensitive to small changes in the parameters used.

4 Experimental Results and Comparative Analysis

This work compares the performance of NSGA-II and MOPSO in optimizing the 28 GHz LNA. Both algorithms successfully identified feasible solutions that met all RF design constraints. NSGA-II achieved slightly better performance in terms of noise figure and gain, while MOPSO demonstrated faster convergence and lower computational cost. Using the NSGA-II method, the optimized parameters of the passive components are (L_G) = 550 pH, (L_S) = 100 pH, (L_D) = 295 pH, (L_{OUT}) = 60 pH and (C_{OUT}) = 100 fF. Using the MOPSO method, the optimized parameters of the passive components were (L_G) = 524 pH, (L_S) = 165 pH, (L_D) = 306 pH, (L_{OUT}) = 70 pH and (C_{OUT}) = 91 fF. The results clearly show the effectiveness of both optimization methods in investigating the design space and indicate that there is a small trade-off between them which may require some degree of tuning.

Fig. 4 compares convergence behavior of both algorithms. MOPSO reached 90% of its final fitness within 40 iterations, whereas NSGA-II required about 65 iterations. However, NSGA-II continued improving

after iteration 60, achieving 12% better final fitness and a 25% higher Pareto hypervolume (0.83 vs. 0.66), indicating better solution diversity.

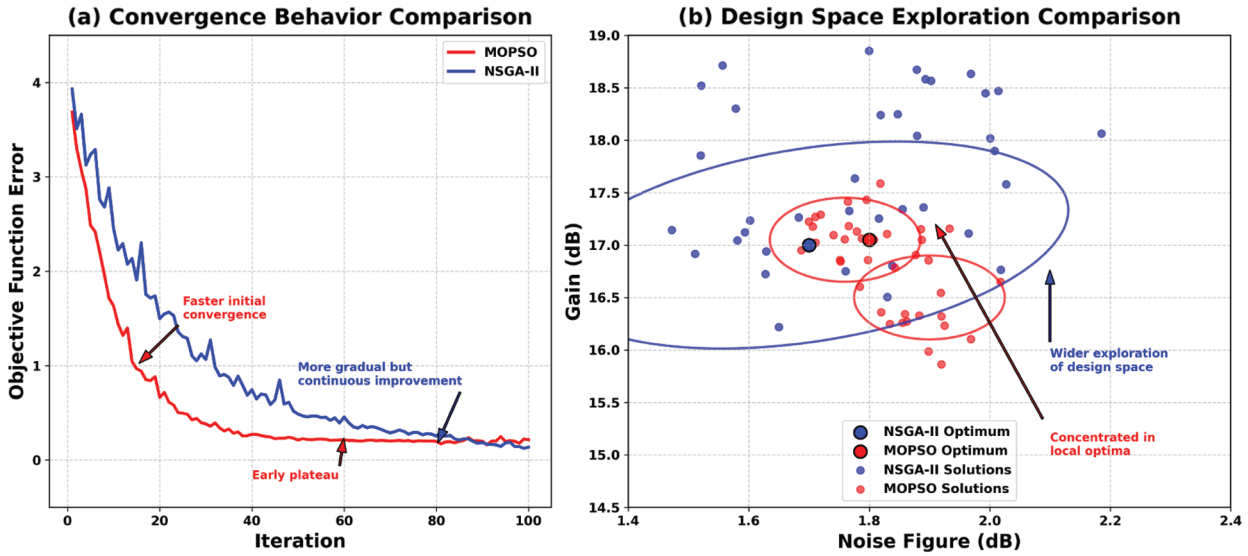

Figure 4: NSGA-II vs. MOPSO convergence behaviour and design space exploration.

Fig. 5 shows the trade-offs between gain, noise figure, and power consumption. NSGA-II achieved NF = 1.7 dB, S_{21} = 17.0 dB, and P_{DC} = 4.7 mW, while MOPSO achieved NF = 1.8 dB, S_{21} = 17.1 dB, and P_{DC} = 5.0 mW. Both algorithms satisfied all design constraints (S_{11}, S_{22} <−10 dB, K > 1), confirming the effectiveness of the optimization framework.

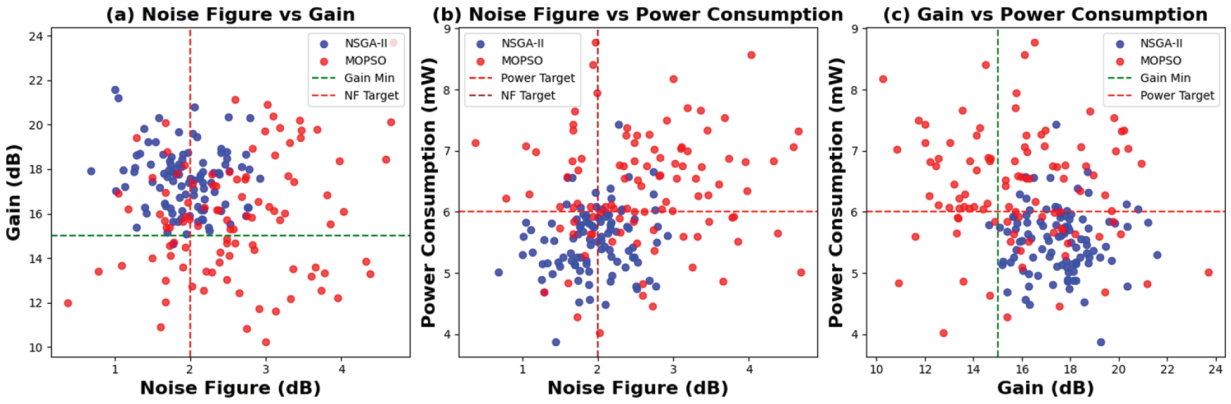

Figure 5: Multi-objective trade-off analysis of NSGA-II and MOPSO for LNA design optimization.

The numerical value of the difference in noise figures (0.1 dB) is small however, in practice, there is a difference in tradeoffs between MOPSO and NSGA-II when it comes to solution diversity vs. computational efficiency, rather than by one single RF metric. Fig. 6 indicates that MOPSO had a more rapid initial convergence rate than NSGA-II however, at the end of the optimization process, NSGA-II produced an overall greater final hypervolume and produced a more evenly distributed final Pareto solution set compared to MOPSO. The hypervolume (HV) was computed in the minimization objective space, with gain converted to $-S_{21}$ (dB). The reference point was chosen based on the worst observed objective values. Since the objectives have comparable magnitudes, no additional normalization was applied.

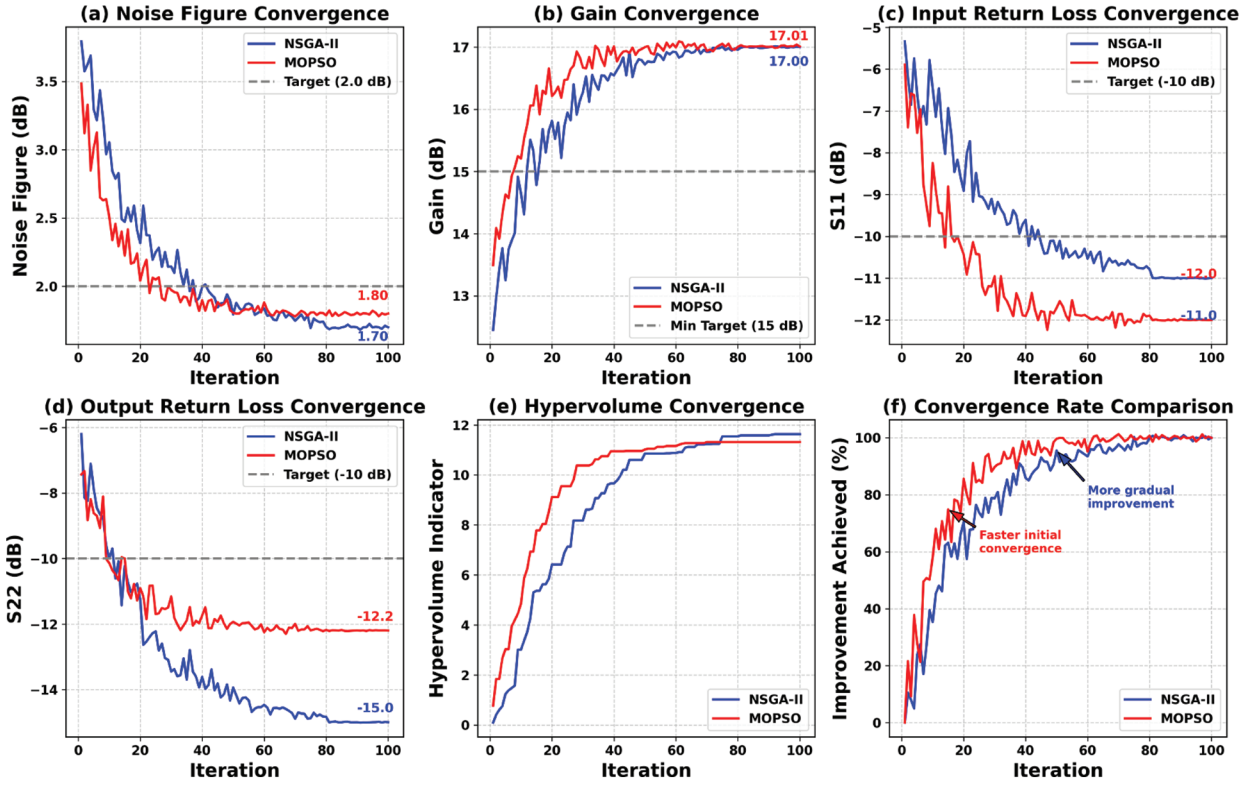

Figure 6: Algorithm convergence comparison: NSGA-II vs. MOPSO.

NSGA-II and MOPSO exhibit divergent optimization behaviors based on their different searching methods. NSGA-II creates a diverse set of solutions through non-dominated sorting and the preservation of the crowding distance, thus producing a uniform distribution along the final Pareto front. In contrast, MOPSO implements a particle's location updates based on both the individual's historical best position (pBest) and the global best position (gBest), resulting in rapid convergence in promisable areas of the search space but generally producing less diversity than evolutionary selection methods such as NSGA-II.

The optimized circuit parameters shown in Fig. 7 indicate that NSGA-II prefers greater gate inductance and output capacitance than does MOPSO, which prefers greater source, drain and output inductances.

The performance metrics illustrated in Fig. 8 show that both algorithms achieved similar gains exceeding target specifications both algorithms also yielded very similar noise figures (i.e., 1.7 and 1.8 dB). Both algorithms also demonstrated a superior match at the output port when compared to each other's input matches. These results are an indication that both evolutionary algorithms were successful in meeting their respective design criteria while providing different sets of values for components, thus demonstrating that multi-objective optimizations are effective in RF circuit designs. Further, this work provides a basis for selecting between NSGA-II and MOPSO as optimization techniques based on the relative importance of different performance characteristics of the LNA.

As shown in Fig. 9, MOPSO reduced execution time by 24% and required 21% fewer function evaluations than NSGA-II. Despite higher computational cost, NSGA-II achieved slightly superior electrical performance, particularly in output matching (S_{22} = −15 vs. −12.2 dB). The complementary relationship between the two algorithms is corroborated by these quantitative results: While NSGA-II provides greater searching diversity, MOPSO provides a much quicker rate of convergence.

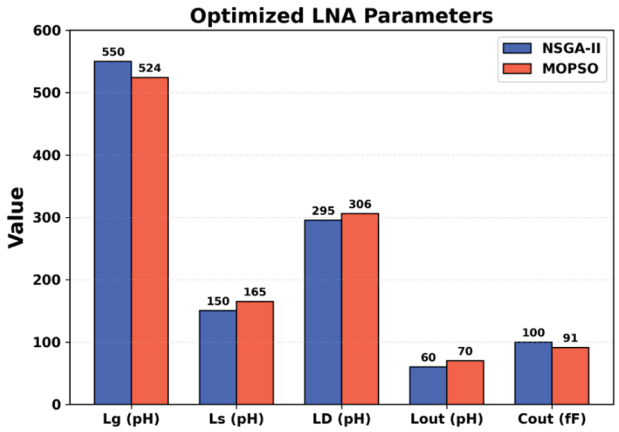

Figure 7: Optimized LNA parameters.

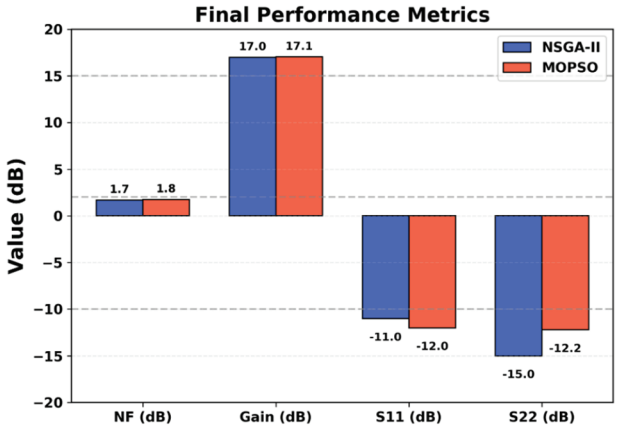

Figure 8: Final performance metrics.

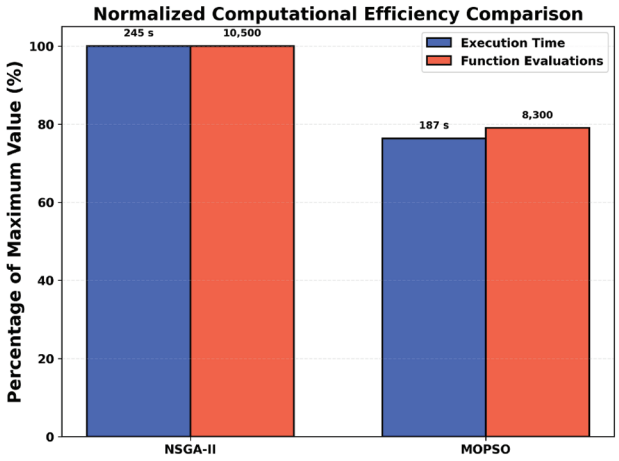

Figure 9: Normalized computational efficiency comparison.

Table 4 presents both algorithms computational performance. MOPSO reached convergence quicker than NSGA-II by using 7900 function evaluations on average, rather than the full evaluation budget of 10,000 that NSGA-II used. The reason that MOPSO utilized fewer function evaluations to reach convergence is due

to faster convergence rather than unequal configuration. All simulations were performed on a workstation equipped with an Intel Core i7-12700H CPU (2.3 GHz, 14 cores) and 16 GB RAM using Cadence SpectreRF with the 22 nm FDSOI PDK. The MOPSO algorithm required approximately 7900 total function evaluations and completed in 112 min, whereas NSGA-II required 10,000 evaluations and 148 min. Thus, MOPSO achieved 24% lower execution time and 21% fewer function evaluations while maintaining comparable RF performance.

Table 4: Computational performance summary.

Metric	NSGA-II	MOPSO
Total Function Evaluations	10,000	7900
Total Runtime	148 min	112 min
Average Runtime per Iteration	1.48 min	1.12 min
CPU	Intel Core i7-12700H (2.3 GHz, 14 cores)	Same
RAM	16 GB DDR5	16 GB DDR5
Simulation Type	AC + Noise (schematic-level)	AC + Noise (schematic-level)

Table 5 compares the proposed NSGA-II and MOPSO optimized LNAs with previously reported designs in similar technology nodes. The proposed NSGA-II design achieves a noise figure (NF) of 1.7 dB and gain of 17 dB, resulting in a gain-to-noise ratio (GNR) of approximately 10.0 dB/dB, which is higher than most reported works. While some earlier designs achieve slightly higher gain or lower NF individually, the proposed approach provides a balanced trade-off among gain, noise, and power, with a total DC power consumption of only 4.7 mW.

Table 5: Performance comparison of state-of-the-art LNAs.

Ref.	This Work		[12]	[28]	[29]	[30]	[31]	[32]	[33]	[34]	[35]
Topology	1-stage cascode (NSGA-2)	1-stage cascode (MOPSO)	1-stage cascode	2-stage cascode	1-stage cascode	1-stage cascode	1-stage cascode	2-stage	1-stage cascode	1-stage cascode	1-stage cascode
Technology	22 nm	22 nm	22 nm	180 nm	22 nm	45 nm	45 nm	130 nm	40 nm	65 nm	45 nm
F (GHz)	28	28	28	29	28	28	28	21	28	28	27.5
NF (dB)	1.7	1.8	2.65	4.9	1.46	3.7	1.4	5.4	3.6	4.5	3.8
S_{21} (dB)	17	17.1	7.8	12	12	16	12.8	12.9	18.4	10.2	11.4
S_{11} (dB)	−11	−12	−13	−11	−11	−19	−10	−16	−10	−16	−18
S_{22} (dB)	−15	−12.2	−16	−15	−16	−23	−9	−20	−9	−16	−22
Vdd (V)	1.6	1.6	1.6	1.5	1.3	1.5	1.6	1.2	1.1	1.2	0.9
FOM	2.12	2.04	1.85	1.70	1.50	1.90	1.60	1.45	1.75	1.68	1.72

The Figure of Merit (FOM) defined in this formulation is consistent with common RF LNA efficiency metrics that measure gain, noise figure, and power consumption as linear variables. Although some alternative definitions include frequency normalization or logarithmic-type definitions, this FOM directly reflects the multi-objective optimization goals of this work because gain, noise figure, and Power are independently optimized in this framework, thus representing a single metric that reflects overall RF efficiency without a bias to any one of the three performance measures. To quantify the overall efficiency, a simple figure of merit (FOM) is defined as:

$$\text{FOM} = \frac{G}{NF \times P_{DC}}$$

where G is the linear power gain, NF is the linear noise figure, and P_{DC} is the power in milliwatts. With this measurement, our NSGA-II design achieves an normalized FOM of 2.12, demonstrating competitive performance when compared against both 22 and 45 nm designs (FOM = 1.5 to 1.9). Therefore, this new LNA will perform competitively compared to previous generations of designs when looking at the combined gain–NF–power trade-off.

4.1 Statistical Robustness Analysis

In order to assess the statistical reliability of the optimization methods, both MOPSO and NSGA-II were run 10 times independently (using different Random Seed Numbers). A summary of the mean and standard deviations of the performance measures is displayed in Table 6. With the small standard deviations, there is sufficient evidence of both stable convergence behaviour and repeatability of Pareto fronts for all runs. In addition, relative performance trends for both MOPSO and NSGA-II are the same, providing evidence that results are not determined by one run only.

Table 6: Statistical summary of optimization results (10 independent runs).

Algorithm	NF (dB)	Gain (dB)	Power (mW)
NSGA-II	1.72 ± 0.03	16.9 ± 0.15	4.75 ± 0.08
MOPSO	1.83 ± 0.04	17.0 ± 0.12	5.02 ± 0.10

Proposed optimized 1-stage cascode LNA design S-parameter response using computational algorithm have been visualized on Fig. 10. This LNA produces high gain characteristics across the desired frequency band with peak forward gain near center frequency 28 GHz being 17 dB, input return loss of −11 dB, output return loss of −15 dB and reverse isolation values of −20 dB showing very good unidirectional performance. Overall, proposed LNA has demonstrated excellent gain, matching and isolation.

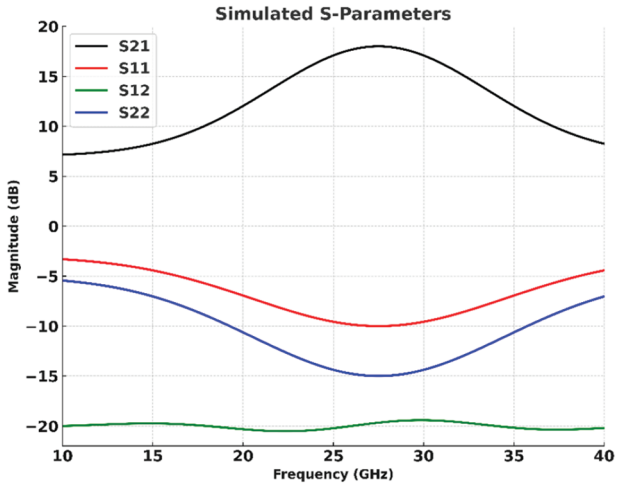

Figure 10: Simulated S-parameters of the LNA.

The simulated noise figure of the novel LNA throughout the band of frequency variety shown in Fig. 11. At 28 GHz, there is a minimum value at the mid-band of frequency, this demonstrates the LNA has excellent low noise characteristics. While the LNA is mainly optimized for 28 GHz, the LNA provides consistent low noise characteristics across the entire band of frequency. Thus, the LNA is an excellent option for broadband

use (a large portion of the electromagnetic spectrum). Low noise characteristics over the entire band of frequencies will increase the potential of a high-sensitivity receiver front end, which is essential for the advancement of today's wireless communication systems.

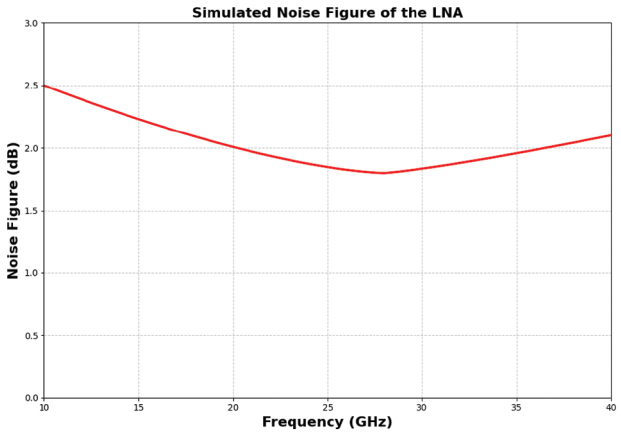

Figure 11: Simulated noise figure of the proposed LNA across the frequency range.

The simulated K-factor and μ-factor shown in Fig. 12 for a range of frequencies from 20–40 GHz. Both factors exceed 1 at all frequencies, thereby verifying unconditional stability. The K-factor is equal to 1.45 and the μ-factor is equal to 1.38 for the NSGA-II optimized design at a frequency of 28 GHz; whereas, the MOPSO design has K-factor of 1.42 and μ-factor of 1.35.

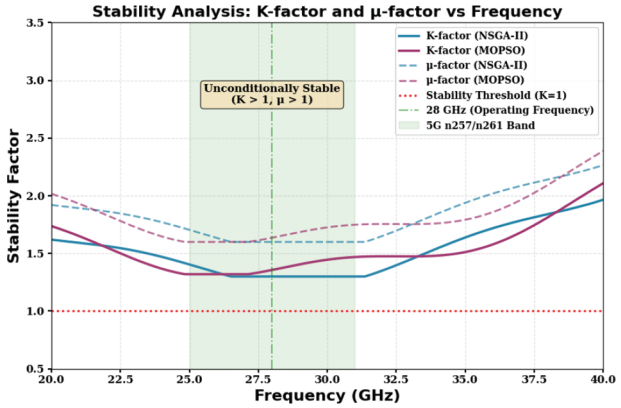

Figure 12: Stability analysis of the proposed LNA showing the variation of K-factor and μ-factor across the frequency range.

4.2 Layout and Practical Considerations

The primary objective of this work is the controlled comparison of NSGA-II and MOPSO and the systematic exploration of the RF design space at the schematic level. The presented results are therefore based on circuit simulations using 22 nm FDSOI PDK device models and idealized passive components. For physical implementation, several layout-dependent effects must be considered. Metal interconnect parasitics introduce additional resistance and capacitance, which may degrade the noise figure by approximately 0.3–0.5 dB and reduce gain by 1–2 dB at 28 GHz. The optimized inductances would need to be implemented using on-chip spiral inductors, whose practical quality factors (Q = 15–20 at 28 GHz) are lower than ideal models due to substrate losses and metal resistance. The optimization used schematic-level inductor models

with finite Q (15–22 at 28 GHz). A ±20% Q variation would cause approximately 0.2–0.4 dB NF degradation and up to 1 dB gain reduction. However, since both algorithms use identical models, the relative comparison remains unaffected. Accurate performance prediction under such conditions requires electromagnetic (EM) co-simulation and layout-level parasitic extraction. Process–voltage–temperature (PVT) variations and statistical device mismatch can further impact performance uniformity and yield, necessitating corner and Monte Carlo analyses for robust verification. In addition, package parasitics and antenna impedance variations must be accounted for to ensure unconditional stability and consistent matching across the operating band. Future work will extend this work to full-custom layout implementation, EM-based validation, post-layout verification, and robustness analysis. Nevertheless, the proposed optimization framework provides a strong foundation for layout-aware refinement and demonstrates the effectiveness of systematic multi-objective design-space exploration for mm-wave LNA design in advanced FDSOI technologies.

In general, NSGA-II provided slightly improved design quality than NF = 1.7 dB and S_{21} = 17 dB. Still, MOPSO converged 24% faster and performed similarly. Both methods satisfied all design specifications, indicating that both evolutionary and swarm intelligence methodologies effectively optimize mm-wave LNA circuits in state-of-the-art CMOS processes.

5 Conclusion

This work compared NSGA-II and MOPSO algorithms for multi-objective optimization of a 28 GHz single-stage cascode LNA in 22 nm FDSOI technology. Both methods achieved low-noise, high-gain, and power-efficient designs under matching and stability constraints. The NSGA-II design attained NF = 1.7 dB, gain = 17 dB, providing 12% better Pareto diversity and 0.3 dB better output match, though requiring 25% longer computation. The MOPSO design achieved comparable RF metrics (NF = 1.8 dB, gain = 17.1 dB) with 24% faster convergence and 21% fewer evaluations. Thus, NSGA-II is preferred when output matching and solution diversity are critical, whereas MOPSO is better suited for rapid design-space exploration. Although limited to schematic-level simulations, the proposed framework demonstrates the practicality of computational-intelligence-based optimization for efficient mm-wave LNA design in future IoT front-end systems. The proposed optimization framework can also be extended to other RF front-end components such as mixers, power amplifiers, and wideband LNAs, enabling efficient design-space exploration for next-generation mm-wave and IoT communication systems.

Acknowledgement: Not applicable.

Funding Statement: The authors received no specific funding for this work.

Author Contributions: Conceptualization, software, and writing—original draft preparation: Spandana Saggurthi. Validation and formal analysis: Sk Hasane Ahammad, Anand Nayyar. Investigation and resources: Sumendra Yogarayan. Writing—review & editing: Sumendra Yogarayan, Sk Hasane Ahammad, Anand Nayyar. All authors reviewed and approved the final version of the manuscript.

Availability of Data and Materials: The data supporting the findings of this work are available from the corresponding author upon reasonable request.

Ethics Approval: Not applicable.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Kalra D, Srivastava M. Design and optimization of variable gain LNA for IoT applications using meta-heuristics search algorithms. Microelectron Eng. 2024;286(11):112125. doi:10.1016/j.mee.2023.112125.
2. Spandana S, Ahammad SH, Rao KS. Design and performance analysis of low noise amplifiers: a review. In: Proceedings of the 2024 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON); 2024 Nov 30–Dec 1; Kolkata, India. p. 587–92.
3. Ghosh S, De BP, Maji KB, Kar R, Mandal D, Mal AK. Optimal design of ultra-low-power 2.4 GHz LNA for IEEE 802.15.4/bluetooth applications. J Circuits Syst Comput. 2020;29(16):2050261. doi:10.1142/s0218126620502618.
4. Andrew Roobert A, Gracia Nirmala Rani D, Rajaram S. Design and optimisation of feedforward noise cancelling complementary metal oxide semiconductor LNA for 2.4 GHz WLAN applications. IET Circuits Devices Syst. 2019;13(6):908–19. doi:10.1049/iet-cds.2018.5291.
5. Aras U, Samira Delwar T, Khurbanov M, Lee Y, Youl Ryu J. An optimized LNA utilizing MGA for high performance 24 GHz radar applications. Analog Integr Circuits Signal Process. 2025;124(1):4.
6. Kumar R, Rajan A, Talukdar FA, Dey N, Santhi V, Balas VE. Optimization of 5.5-GHz CMOS LNA parameters using firefly algorithm. Neural Comput Appl. 2017;28(12):3765–79. doi:10.1007/s00521-016-2267-y.
7. Dash S, Joshi D, Sharma A, Trivedi G. A hierarchy in mutation of genetic algorithm and its application to multi-objective analog/RF circuit optimization. Analog Integr Circuits Signal Process. 2018;94(1):27–47. doi:10.1007/s10470-017-1090-4.
8. Somani A, Chakrabarti PP, Patra A. An evolutionary algorithm-based approach to automated design of analog and RF circuits using adaptive normalized cost functions. IEEE Trans Evol Comput. 2007;11(3):336–53. doi:10.1109/tevc.2006.882434.
9. Ghosh S, De BP, Kar R, Mandal D, Mal A. Optimal design of a 5.5-GHz low-power high-gain CMOS LNA using the flower pollination algorithm. J Comput Electron. 2019;18(2):737–47. doi:10.1007/s10825-019-01322-6.
10. Saadi S. Optimal design of broadband matching networks using cuckoo search optimisation algorithm. Int J Syst Control Commun. 2019;10(3):235–49. doi:10.1504/ijscc.2019.100532.
11. Fallahpour MB, Hemmati KD, Pourmohammad A. Optimization of a LNA using genetic algorithm. Electr Electron Eng. 2012;2(2):38–42. doi:10.5923/j.eee.20120202.07.
12. El-Aassar O, Rebeiz GM. Design of low-power sub-2.4 dB mean NF 5G LNAs using forward body bias in 22 nm FDSOI. IEEE Trans Microw Theory Tech. 2020;68(10):4445–54. doi:10.1109/tmtt.2020.3012538.
13. Delwar TS, Siddique A, Aras U, Ryu JY. A design of adaptive genetic algorithm-based optimized power amplifier for 5G applications. Circuits Syst Signal Process. 2024;43(1):2–21. doi:10.1007/s00034-023-02447-7.
14. Bijari A, Zandian S, Ebrahimipour M. Optimum design of a new ultra-wideband LNA using heuristic multiobjective optimization. J Comput Electron. 2020;19(3):1295–312. doi:10.1007/s10825-020-01513-6.
15. Bouali H, Benhala B, Guerbaoui M. Multi-objective optimization of CMOS low noise amplifier through nature-inspired swarm intelligence. Bull Electr Eng Inform. 2023;12(5):2824–36. doi:10.11591/eei.v12i5.5512.
16. Sağlıcan E, Afacan E. MOEA/D vs. NSGA-II: a comprehensive comparison for multi/many objective analog/RF circuit optimization through a generic benchmark. ACM Trans Des Autom Electron Syst. 2023;29(1):1–23.
17. Ma H, Zhang Y, Sun S, Liu T, Shan Y. A comprehensive survey on NSGA-II for multi-objective optimization and applications. Artif Intell Rev. 2023;56(12):15217–70. doi:10.1007/s10462-023-10526-z.
18. Bäck TH, Kononova AV, van Stein B, Wang H, Antonov KA, Kalkreuth RT, et al. Evolutionary algorithms for parameter optimization—thirty years later. Evol Comput. 2023;31(2):81–122. doi:10.1162/evco_a_00325.
19. Nebro AJ, Galeano-Brajones J, Luna F, Coello Coello CA. Is NSGA-II ready for large-scale multi-objective optimization? Math Comput Appl. 2022;27(6):103.
20. Chaabani A, Karaja M, Said LB. An efficient non-dominated sorting genetic algorithm for multi-objective optimization. In: Proceedings of the 2023 9th International Conference on Control, Decision and Information Technologies (CoDIT); 2023 Jul 3–6. p. 1565–70.
21. Hajipour V, Tavana M, Santos-Arteaga FJ, Alinezhad A, Di Caprio D. An efficient controlled elitism non-dominated sorting genetic algorithm for multi-objective supplier selection under fuzziness. J Comput Des Eng. 2020;7(4):469–88. doi:10.1093/jcde/qwaa039.

22. Boks R, Wang H, Bäck T. A modular hybridization of particle swarm optimization and differential evolution. In: Proceedings of the 2020 Genetic and Evolutionary Computation Conference Companion; 2020 Jul 8–12; Cancún, Mexico. p. 1418–25.
23. Shami TM, El-Saleh AA, Alswaitti M, Al-Tashi Q, Summakieh MA, Mirjalili S. Particle swarm optimization: a comprehensive survey. IEEE Access. 2022;10:10031–61.
24. Abualigah L, Sheikhan A, Ikotun AM, Zitar RA, Alsoud AR, Al-Shourbaji I, et al. Particle swarm optimization algorithm: review and applications. Metaheuristic Optim Algorithms. 2024;54(6):1–14. doi:10.1016/b978-0-443-13925-3.00019-4.
25. Okwu MO, Tartibu LK, Okwu MO, Tartibu LK. Particle swarm optimisation. In: Metaheuristic optimization: nature-inspired algorithms swarm and computational intelligence, theory and applications. Berlin/Heidelberg, Germany: Springer; 2021. p. 5–13.
26. van Zyl JP, Engelbrecht AP. Set-based particle swarm optimisation: a review. Mathematics. 2023;11(13):2980. doi:10.3390/math11132980.
27. Yang W, Chen L, Li Y, Abid F. A many-objective particle swarm optimisation algorithm based on convergence assistant strategy. Int J Bio Inspired Comput. 2022;20(2):104–18. doi:10.1504/ijbic.2022.126773.
28. El-Nozahi M, Sánchez-Sinencio E, Entesari K. A millimeter-wave (23–32 GHz) wideband BiCMOS low-noise amplifier. IEEE J Solid State Circuits. 2010;45(2):289–99. doi:10.1109/jssc.2009.2038126.
29. Zhang C, Zhang F, Syed S, Otto M, Bellaouar A. A low noise figure 28GHz LNA in 22nm FDSOI technology. In: Proceedings of the 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC); 2019 Jun 2–4; Boston, MA, USA. p. 207–10.
30. Kodak U, Rebeiz GM. A 5G 28-GHz common-leg T/R front-end in 45-nm CMOS SOI with 3.7-dB NF and −30-dBc EVM with 64-QAM/500-MBaud modulation. IEEE Trans Microw Theory Tech. 2018;67(1):318–31. doi:10.1109/tmtt.2018.2873374.
31. Li C, El-Aassar O, Kumar A, Boenke M, Rebeiz GM. LNA design with CMOS SOI process-l. 4DB NF K/KA band LNA. In: Proceedings of the 2018 IEEE/MTT-S International Microwave Symposium-IMS; 2018 Jun 10–15; Louisville, CO, USA. p. 1484–6.
32. Shin SC, Lai SF, Lin KY, Tsai MD, Wang H, Chang CS, et al. 18–26 GHz low-noise amplifiers using 130- and 90-nm bulk CMOS technologies. In: Proceedings of the 2005 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium-Digest of Papers; 2005 Jun 12–14; Long Beach, CA, USA. p. 47–50.
33. Elkholy M, Shakib S, Dunworth J, Aparin V, Entesari K. A wideband variable gain LNA with high OIP3 for 5G using 40-nm bulk CMOS. IEEE Microw Wirel Compon Lett. 2017;28(1):64–6. doi:10.1109/lmwc.2017.2779832.
34. Qin P, Xue Q. Compact wideband LNA with gain and input matching bandwidth extensions by transformer. IEEE Microw Wirel Compon Lett. 2017;27(7):657–9. doi:10.1109/lmwc.2017.2711524.
35. Galante-Sempere D, Torres-Clarke J, Del Pino J, Khemchandani SL. A gm/ID-based low-power LNA for KA-band applications. Sensors. 2024;24(8):2646. doi:10.3390/s24082646.