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High Precision SAR ADC Using CNTFET for Internet of Things

V. Gowrishankar[1, *] and K. Venkatachalam[1]

Abstract: A high precision 10-bit successive approximation register analog to digital converter (ADC) designed and implemented in 32nm CNTFET process technology at the supply of 0.6V, with 73.24 dB SNDR at a sampling rate of 640 MS/s with the average power consumption of 120.2 μW for the Internet of things node. The key components in CNTFET SAR ADCs are binary scaled charge redistribution digital to analog converter using MOS capacitors, CNTFET based dynamic latch comparator and simple SAR digital code error correction logic. These techniques are used to increase the sampling rate and precision while ensuring the linearity, power consumption and noise level are within the limit. The proposed architecture has high scalability to CNTFET technology and also has higher energy efficiency. We compared the results of CNTFET based SAR ADC with other known architectures and confirm that this proposed SAR ADC can provide higher precision, power efficiency to the Internet of things node.

Keywords: Internet of things, CNTFET, successive approximation register ADC, signal to noise and distortion ratio, MOS capacitor.

1 Introduction

The Internet of Things (IoT) has been one of the most emerging technologies in today's daily life. Their applications include smart home, smart cities, smart grid, connected health, industrial internet, smart wearable and smart farming. Without an analog to digital converter, the Internet of Things would be a just science fiction fantasy. The IoT nodes need to be compact, low power and portable one. An ADC which are integrated into IoT nodes is needed to digitize analog sensor data for digital signal processing, storage and transmission. In IoT applications, the precision and the sampling rate of the ADCs need to be wide and configurable to cope with different analog sensors used. Due to power consumption factor, early IoT ADCs are only optimized for low power consumption by sacrificing the speed and accuracy down to the acceptable levels [Ding, Harpe, Chen et al. (2018); Harpe, Gao, Dommele et al. (2016)]. For analog sensors, some applications require on-demand conversion, for instance in case of humidity, light intensity, force, pressure and temperature monitoring. Most of the IoT node sensors require ADC with low resolution and a sampling rate around a few Kilo samples per second but some bio-sensors, motion sensors, accelerometers and image sensors could require a very high sampling rate with higher resolutions in Shim et al. [Shim, Kim, Hong et al. (2018)]. This paper focuses on

[1] Department of ECE, Velalar College of Engineering and Technology, Erode, 638012, India.

[*] Corresponding Author: V. Gowrishankar. Email: shankargow@gmail.com.

successive approximation register ADC, a popular architecture for IoT nodes due to their small form factor and very high power-efficiency as most of the IoT nodes are battery operated. In IoT nodes, analog to digital converters is needed in two locations one in the receiver module and another in the sensor interface stage as shown in Fig. 1.

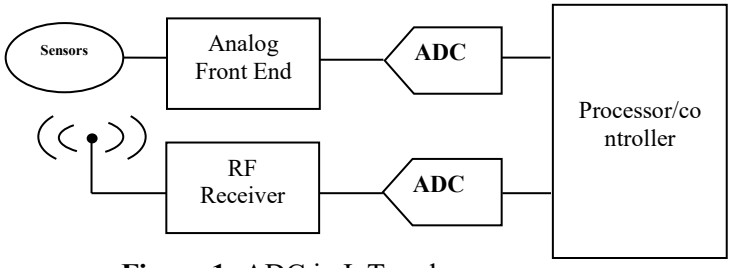

Figure 1: ADC in IoT nodes

The ADCs in IoT nodes are often operated on demand and for a short time only. The SAR ADC architecture has low standby power consumption and instantaneous conversion when compared with other architectures. The resolution of SAR ADCs ranges from 8 to 12 bits and it can achieve higher resolutions by sacrificing the conversion speed. Although early SAR ADCs were designed to use at low speed, low power applications this could lead to suboptimal sensor performance. Recent research works have moved to higher precision with a higher sampling rate for IoT applications. Fortunately, growth in transistor technologies with the introduction of the FinFET, CNTFET process enabled this demand in IoT [Wang and Shi (2018)].

2 SAR ADC architecture

An overview of SAR ADC architecture is shown in Fig. 2. The traditional low power SAR ADC architecture has binary weighted capacitive DAC array, analog comparator, input sampling switch and SAR decision logic. The time interleave techniques have increased the sampling rate of SAR ADCs to GHz range with an increase in the area, power consumption [Stepanovic and Nikolic (2013); Janssen, Doris, Zanikopoulos et al. (2013); Chan, Zhu, Sin et al. (2012); Cao, Yan and Li (2008)]. Smart wearable devices require higher precision ADCs with ultra low power consumption. However, high-precision SAR ADCs are difficult to design because of the comparator's input referred noise limitation as they increase with the number of bits. The pure SAR ADCs operating sampling rate still limited to few Mega samples per second and slowest for high resolution moreover, KT/C-noise from DAC control switches connecting reference voltages to comparator limits the speed and precision of ADC. So far, high power consumption is often used to overcome the noise limitations [Lin, Liu, Huang et al. (2013); Liang, Chen, Han et al. (2014)]. In Hurrell et al. [Hurrell, Lyden, Hummerston et al. (2010)] high SNDR of 90 dB is achieved by amplifying residue charge with power consumption of 105mW at a sampling rate of 12.5 MS/s. In Liu et al. [Liu, Kuo, Lin et al. (2015)] the SNR and SFDR Enhancement Technique called Adaptive tracking average scheme to achieve peak SNDR of 69 dB with an increase in chip area at the supply of 1.2V. In Polineni et al. [Polineni, Bhat, Rajan et al. (2019)], the differential MSB capacitor split switching scheme for digital to analog convertor to improve the SNDR to

55.93 dB with the average power consumption of 337.66 nW at the supply voltage of 0.5V. In recent research, some SAR ADC can achieve 70 dB SNDR with higher energy efficiency. In addition to the input referred noise limitation, capacitor mismatch errors of DAC also affect the precision of SAR ADC. The mismatch errors generate spurious frequency on the ADC output spectrum and cause high degradation to SFDR value. An *N*-bit pure SAR ADC takes *N* comparison cycles for a complete conversion of sampled analog value. To overcome this above limitation, a CNTFET transistor based SAR ADCs with higher sampling rate and a higher precision have been proposed with minimal hardware complexity.

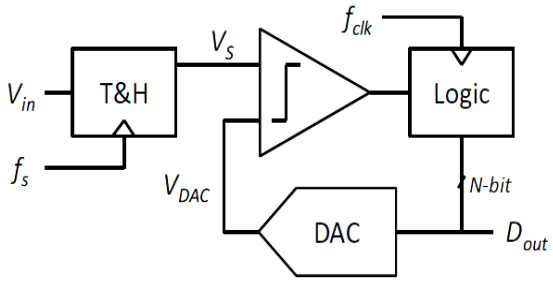

Figure 2: SAR ADC architecture

The paper is organized as follows. Section II discusses carbon nanotube (CNT)-FETs transistors. Section III describes the proposed high performance and low offset voltage CNTFET Comparator. Section IV describes capacitor array digital to analog converter. Section V presents the proposed high precision binary weight CNTFET based SAR ADC. The measured results and analysis are shown in Section VI. Section VII shows the conclusion of the work.

3 Carbon nanotube (CNT)-FET transistor

The scaling down of planar and FinFET transistor dimensions leads to new challenges in the design process such as the short channel effect, very high leakage current, difficulty in gate control and higher power density. Because of the behavioral similarities to planar CMOS transistors and the availability of P-type and N-type transistors, the carbon nanotube field effect transistor (CNTFET) is the better alternative option to replace planar CMOS Transistors and FinFET transistors in Rezaeikhezeli et al. [Rezaeikhezeli, Moaiyeri and Jalali (2013)]. Carbon NanoTube Field Effect Transistors are transistors that their channels are made of new molecular material called carbon nanotube. Due to their ability to work on the nanometer scale, their designs lead to a reduction in form factor and power consumption of IoT nodes. Because of their higher carrier mobility and ballistic conduction, they are the suitable higher speed of operation when compared to planar CMOS transistors. CNTFET is capable of lowering the supply voltage beyond the limit of the CMOS process. CNTFET helps ADCs to reach a higher sampling rate with little noise and distortion effects. Thus, the precision of the CNTFET SAR ADC improved largely when compared with the existing architecture.

4 High performances and low offset voltage CNFET based two stages dynamic comparator

The analog comparators are used to convert the sampled analog sensor value to a quantized single bit. The imperfections in comparator are due to input referred noise, higher offset voltage and larger propagation delay. With technologies scaling, planar and FinFET transistor feature size reduces which leads to the higher offset voltage. The proposed CNTFET comparator with dynamic logic style provides a performance improvement of reduced propagation delay, ultra low supply voltage operation and lower offset voltage. The proposed comparator works in two phases, the pre-amplification phase and the latch regeneration phase. The schematic of CNTFET based dynamic latched comparator is shown in Fig. 3. This structure has separate input and output stages results in lower offset voltage, reduced input referred noise and also zero static power consumption. The preamplifier stage is the p-type differential pair which compares two analog signals to give a current value based on the difference of input voltages. The second stage is the latch regeneration stage that the final output is obtained here depending on the conduction of the preamplifier stage.

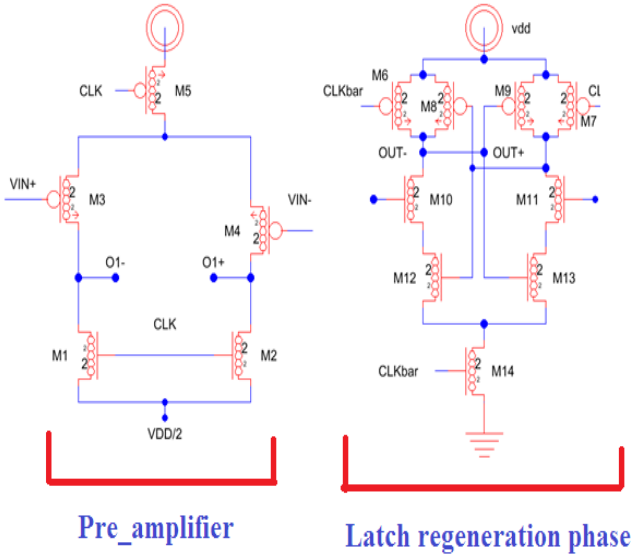

Figure 3: Schematic of the proposed two-stage dynamic CNTFET comparator

In the preamplifier phase, the output node voltages of the first stage are charged to $V_{DD}/2$ which keeps the next latch regeneration stage in active. In order to make zero static power consumption in the next latch stage during the preamplifier phase, a tail transistor is placed in the path of supply voltage V_{DD} to ground. The power consumption of the preamplifier stage is the dominant of total power consumed by the SAR ADC. When the clock becomes high, the comparator will be in the pre-amplification phase. The potential difference between the output nodes of the first stage will be detected by the dynamic latch as soon as NCNFET starts to conduct.

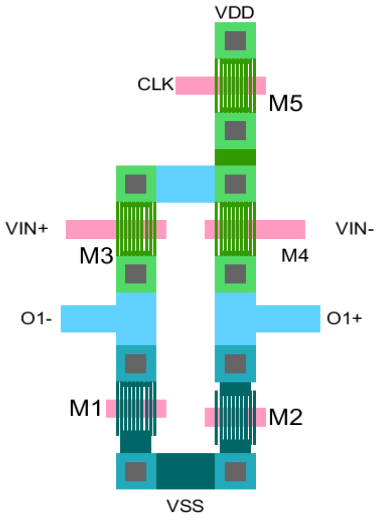

Figure 4: The Layout of the proposed CNTFET preamplifier

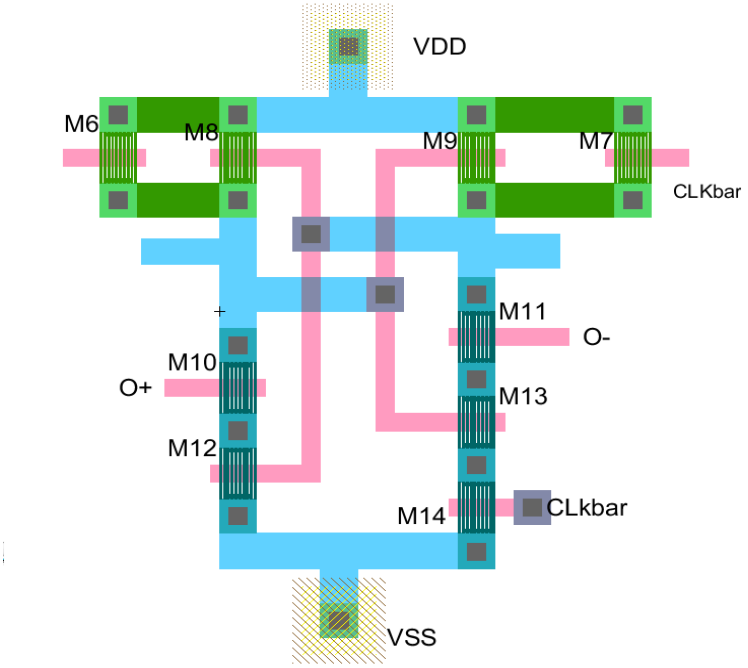

Figure 5: The Layout of proposed CNTFET dynamic latch regeneration

The final digital output is obtained in the regeneration phase. At the beginning of the regeneration phase, the output node voltage of the first stage should be large enough to initiate the positive feedback mechanism in the dynamic latch. This faster mechanism reduces the delay of the latch stage significantly. The improvement in the performance of a CNTFET pre-amplifier and the dynamic latch speeds up the comparator significantly compared to the planar CMOS and FinFET comparators. Fig. 4 and Fig. 5 display the layout of the proposed

CNTFET Preamplifier and the layout of CNTFET dynamic latch regeneration.

Reduced transistor mismatch errors such as threshold voltage, parasitic node capacitance led to the lower offset voltage of the comparator. Fortunately, the CNTFET comparator reduces the decision time and the power consumption largely so the size of input CNTFET transistors can be modified to reduce the input referred noise of the preamplifier stage. The proposed CNTFET comparator has also zero static power consumption. Hence it is excellent power efficiency. Fig. 6 shows the simulation result for the proposed CNTFET based dynamic latch comparator.

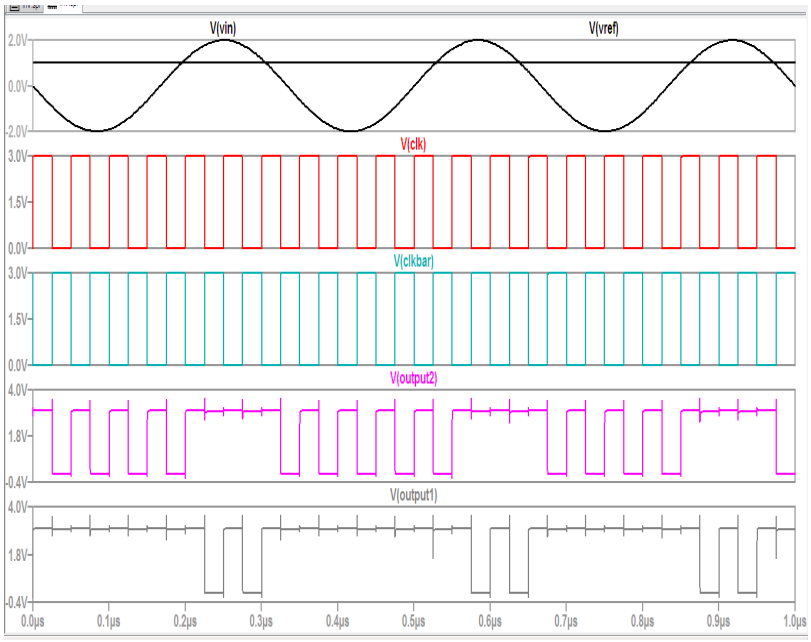

Figure 6: Simulation result for proposed dynamic CNTFET comparator

5 Capacitor digital to analog converter

Fig. 7 is the proposed high precision binary weighed CNTFET SAR ADC architecture. The First stage SAR ADC consists of binary weighted Capacitive array DAC (CDAC) which act as an input sampling capacitor to the reduce capacitance mismatch error and to save the area of ADC device and it uses monotonic switching scheme. The CDAC consists of upper and the lower capacitor array which results in the reduction of a number of capacitors. The speed or settling time, the size of the DAC capacitors has to be reduced. The proposed system utilizes a metal-oxide-semiconductor capacitor instead of a normal metal capacitor as it requires less area, a reduced number of masking layers during the device fabrication process without a decrease in the precision of ADC.

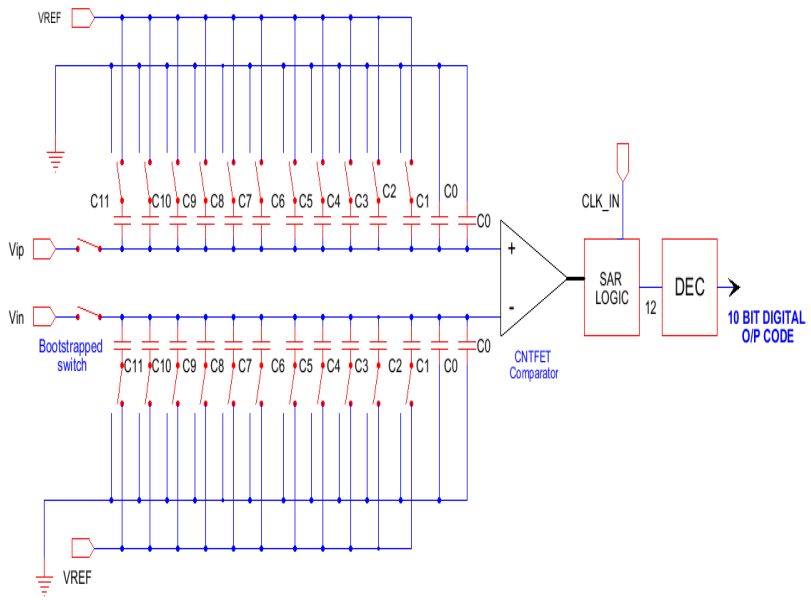

Figure 7: Architecture of proposed differential SAR ADC

6 Proposed high precision binary weighed CNFET SAR ADC

For an existing N bit SAR ADC, it needs several comparison clocks cycles for converting an analog sensor value to N-bit digital output code. The total capacitance C_{Total} of the DAC capacitor array is $2^N C_0$. C_0 is the unit capacitor and V_{REF} is the reference voltage. The proposed high precision IoT SAR ADC samples the sensor analog signal through bootstrapped switches at the top plates of the MOS capacitor array. When the bootstrapped switches are on state and ADC is in sampling mode. The bottom plates of the capacitor array are initially connected to the ground. The coupling effect degrades the IoT ADC performances to reduce these effects we use metal-oxide-semiconductor field effect capacitors. The digital binary code from SAR logic is used to control the switch of the bottom plate capacitor between V_{REF} and ground. The conversion starts by switching the bottom plate of the capacitor array from LSB to MSB capacitors to V_{REF} or to the ground according to SAR logic. After the DAC output has settled to its new value, the comparator is strobe again and the new sequence is repeated. The SAR digital code error correction circuit converts the redundant 12-bit digital output code to 10-bit code. The SAR digital code error correction circuit consists of full adders, CNTFET flip flops and multiplexers. When the skip signal is set to logic high, the last conversion cycle is neglected and the number of conversion steps is reduced to 10. At the end of the last clock cycle, a resultant digital bit loaded into register and control logic resets again.

7 Measurement results

The proposed high precision SAR ADC was designed in 32 nm CNTFET technology. The ADC device occupies an area of 28 μm×30 μm. it is different from the research works of Liu et al. [Liu, Chun, Kuo et al. (2015); Polineni, Bhat and Rajan (2019); Kull, Luu,

Menolfi et al. (2018)] in achieving a higher sampling rate. The prototype high precision SAR ADC uses the supply voltage of from 0.6V to 0.9V. For testing the dynamic characteristics sinusoidal signal of a frequency of 15 MHz is applied and Simulation results show that the peak Differential Non-Linearity is +0.16/-0.12 LSB, and Integral Non-Linearity is +0.20/-0.14 LSB with the perfect matched binary capacitor array. Fig. 8 and Fig. 9 show the INL and DNL errors and ENOB of the proposed SAR ADC. The power spectral density near Nyquist frequency is shown in Fig. 10. The measured SNDR is 73.24 dB, and the average effective number of bits is 9.2 bits. Fig. 11 displays speed improvement versus supply voltage. Tab. 1 shows a Performance comparison and specification to the prior work.

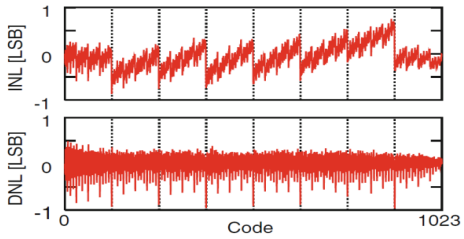

Figure 8: Measured INL and DNL errors of SAR ADC

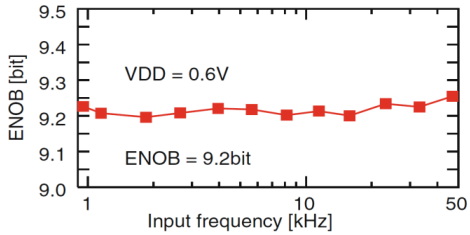

Figure 9: Effective Number of bits [ENOB] of ADC

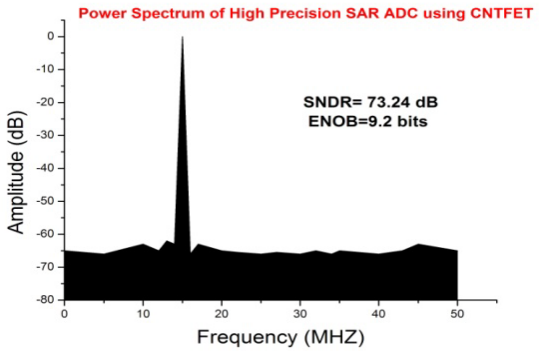

Figure 10: Spectral analysis of SAR ADC digital output

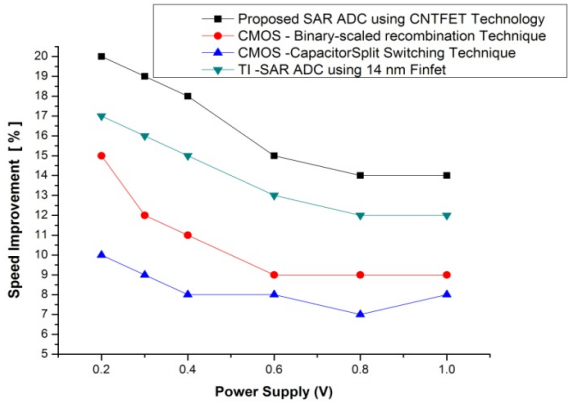

Figure 11: Power supply *vs.* speed improvement

Table 1: Performance comparison and specification summary

Source	[Liu (2015)]	[Polineni (2019)]	[Kull (2018)]	This Work
Technology [nm]	20nm	90nm	14 nm FinFET	32 nm CNTFET
Sampling rate [mega sample/s]	160	615	800	640
Resolution	10	10	10	10
ENOB	9.1	9	7.1	9.2
Supply voltage [V]	0.9	0.5	0.9	0.6
DNL [in LSB]	-0.34/0.41	0.3/-0.34	0.3/-0.34	+0.16/-0.12
INL [in LSB]	-0.43/0.28	0.3/-0.34	0.3/-0.34	+0.20/-0.14
SNDR [dB]	57.7	55.93	40.9	73.24
Power [μW]	150	110	235	120.2

8 Conclusions

In this work, a binary weight-based charge redistribution DAC SAR ADC using CNTFET process technology to overcome the problem of low precision and the low sampling rate is present. By optimizing comparator design using CNTFET transistor and designing charge sharing capacitor array using metal-oxide-semiconductor capacitor. The prototype of SAR ADC achieves 640 MS/s operation speed with ENOB of 9.2 bit for 10-bit resolution. The measured results demonstrate that ADC linearity parameters INL and DNL are within the specified range and also due to the low leakage current of CNTFET transistors power efficiency increases and makes it suitable for the Internet of things.

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