Computer Modeling in Engineering & Sciences

Tech Science Press

https://doi.org/10.32604/cmes.2026.083270

ARTICLE

A Unified Physics-of-Failure Framework for Reliability Prediction of SiC MOSFET Inverters under Stochastic Mission Profiles

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Received: 31 March 2026; Accepted: 01 June 2026; Published: 27 July 2026

ABSTRACT: Silicon Carbide Metal Oxide Semiconductor Field Effect Transistors (SiC MOSFETs) have superior characteristics compared to traditional Silicon-based switching devices. SiC devices can support fast switching speeds and high blocking voltages. Due to limited historical data and rapid technological improvements, there is not enough field data to correctly evaluate the reliability of the state-of-the-art SiC MOSFETs. An accurate model of their reliability and aging characteristics is needed to expedite their rapid commercial adoption in mission-critical applications, such as offshore wind farms and electric vehicles. Classical handbook-based methods produce large errors due to their inability to correctly account for the long-term device parameter variation of new technologies. This paper proposes a versatile model-based approach to study the SiC MOSFET based three-phase inverters under various mission profiles. The proposed framework combines electrical, thermal, and aging (ET&A) models to emulate the SiC MOSFET device parameter variations and their amplifying effect on the aging phenomenon. Unlike existing approaches, the proposed framework captures the coupled electrothermal–aging feedback and progressive parameter variation under stochastic mission profiles, enabling more accurate long-term reliability prediction. The model can be adopted in Monte-Carlo simulations to predict the reliability of three-phase inverters under application-specific stochastic mission profiles. The accuracy of the aging models is tested by comparing the results against accelerated lifetime test data obtained from the literature. An example case study is presented to demonstrate the application of the proposed ET&A models to predict the reliability of wind turbine inverters considering mission profile data from a wind farm site in northwest Taiwan.

KEYWORDS: Failure mechanisms; on-state resistance aging; reliability prediction; SiC MOSFET; three-phase inverter

1 Introduction

Power devices have evolved through several generations, from conventional Silicon (Si) devices to wide-bandgap (WBG) technologies such as Silicon Carbide (SiC) and Gallium Nitride (GaN). Compared with Si devices, SiC MOSFETs can sustain higher blocking voltages, achieve faster switching, and operate at elevated junction temperatures, enabling high-efficiency and high-power-density power converters for mission-critical applications such as offshore wind farms and electric vehicles [1,2].

Despite these advantages, the reliability of state-of-the-art SiC MOSFETs remains difficult to quantify accurately because the technology is evolving rapidly and has limited long-term field history [1,2]. At the same time, the economic and safety consequences of unexpected power-electronic failures can be severe. In particular, inverter downtime in offshore renewable plants can trigger costly corrective maintenance and reduced availability; accurate lifetime prediction is therefore needed at the planning stage [1,3].

A central challenge is that inverter stresses are not constant. Renewable-energy converters experience time-varying load demand and ambient-temperature variations, which generate junction-temperature cycling and intermittent exposure to high peak temperatures. Moreover, high-resolution variability (e.g., turbulence-driven fluctuations) can materially increase thermal stress and fatigue compared with average-profile assumptions [4–7]. Consequently, reliability prediction requires models that relate mission-profile-driven electrothermal stresses to progressive degradation, rather than assuming time-invariant device characteristics [1–3].

1.1 Degradation and Failure Mechanisms Relevant to Long-Term Reliability

Fig. 1 showcases the dominant failure mechanism of SiC-MOSFET. When junction temperature and blocking voltage remain below critical values, catastrophic avalanche-induced failures can largely be avoided; however, long-term degradation can still occur through fatigue-induced chip- and packaging-related mechanisms [1,2,8]. Chip-level degradation refers to gradual changes in the electrical properties of the SiC MOSFET die (e.g., gate-oxide defect accumulation, drift-region resistance changes), whereas package-level degradation includes bond-wire fatigue and solder/attach degradation driven by thermomechanical stresses associated with Coefficient-of-Thermal-Expansion (CTE) mismatch [2,9]. Recent studies have further highlighted the role of multi-stress-induced degradation and complex package-level failure mechanisms in SiC MOSFETs, emphasizing the coupled nature of electrical, thermal, and mechanical aging processes [10,11].

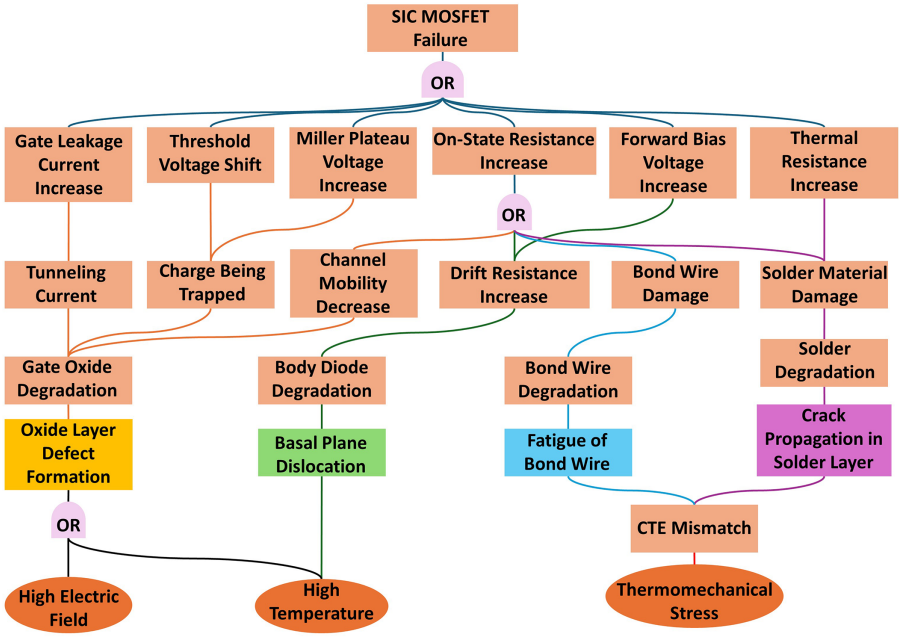

Figure 1: SiC MOSFET fault tree analysis summarizing the main failure mechanisms.

Operational stresses lead to aging, which manifests as drift in key electrical parameters. Excessive deviations can reduce converter efficiency and eventually violate design constraints, at which point the device is considered to have reached the end of useful life. Recent experimental studies have analyzed the evolution of electrical model parameters during power cycling, confirming that multiple degradation mechanisms contribute to observable parameter drift such as on-state resistance increase [12].

Among candidate health indicators, the on-state drain–source resistance (R_{dson}) is particularly relevant for long-term modeling because it is affected by multiple dominant degradation pathways and directly

impacts conduction losses and thermal loading. Gate-oxide degradation can increase threshold voltage (V_{th}), R_{dson}, leakage currents ($I_{g,lk}$, $I_{ds,lk}$), and Miller plateau voltage [13–15]. Body-diode degradation and package-related degradation (bond-wire lift-off, delamination, solder fatigue) can further increase R_{dson} and thermal resistance, raising junction temperature and accelerating aging [1,3,5].

Because these mechanisms are coupled through temperature, R_{dson} provides a practical bridge between degradation physics and converter-level electrothermal behavior. Modeling R_{dson} drift supports long-term planning questions such as lifetime distributions under stochastic mission profiles and the impact of operational policies that reduce temperature swings [3,16]. Although multiple degradation mechanisms are illustrated in Fig. 1, many of these effects ultimately manifest as an increase in conduction path resistance, either directly or indirectly. Therefore, R_{dson} is adopted as a unified system-level indicator to capture the combined impact of the dominant degradation pathways.

1.2 Prior Reliability Approaches and Their Limitations

Existing reliability prediction approaches for power devices can be broadly grouped into three categories: (i) handbook-based constant failure-rate models, (ii) accelerated life test (ALT)-driven empirical models, and (iii) condition-monitoring/prognostic approaches. While each category offers useful insights, none directly provides a computationally efficient, physics-consistent way to predict long-horizon inverter reliability under stochastic mission profiles and aging-induced parameter drift.

i. Handbook and constant-failure-rate models: Classical reliability prediction has historically relied on handbook methods that assume constant failure rates. Such approaches are increasingly inadequate for modern electronics, including WBG devices, because they do not account for progressive parameter drift and changing failure propensity with age, which can yield optimistic lifetime estimates under variable loading [3,17].

ii. Accelerated life tests (ALTs): Accelerated testing can characterize failure modes and estimate their statistical distributions under controlled stress conditions. For SiC MOSFETs, commonly used ALT methodologies include thermal cycling (TC), DC power cycling (DC-PC), AC power cycling (AC-PC), high-temperature gate bias (HTGB), high-temperature gate switching (HTGS), and chopper-mode bias (CMB) [2,13,15,18]. Although ALT-based approaches are theoretically sound, they are expensive and time-consuming and often difficult to map to field operation when mission profiles are highly variable and involve multi-stressors. This limits their practicality for rapidly evolving SiC technologies and can lead to poor correlation with real converter stresses [17,18]. Recent work has therefore proposed inverter-like accelerated tests designed to emulate inverter operating conditions more closely; such studies report that degradation behavior and lifetime evaluation can differ compared with conventional power cycling tests, underscoring the need for realistic stress representation [19].

iii. Condition monitoring and short-horizon prognosis: Converter reliability can also be improved through protection design and device condition monitoring. Continuous junction-temperature monitoring is especially important for safe SiC MOSFET operation, and both direct sensor-based methods and indirect methods based on temperature-sensitive electrical parameters (TSEPs) have been proposed [15,20–23]. Common TSEPs include V_{th}, R_{dson}, $I_{g,lk}$, internal gate resistance ($R_{g,int}$), and forward body-diode voltage (V_{bd}). However, many TSEPs are also age dependent; ignoring aging can bias temperature estimation and may lead to junction-temperature underestimation [15,24,25]. Certain precursors (e.g., sharp rises in gate leakage current) can indicate imminent failure and are useful for short-horizon prognosis [26–28]. Condition monitoring therefore serves a different objective than long-term planning: it aims to predict near-term failures using real-time measurements and ALT-informed

mappings, whereas long-term converter design requires predicting aging trajectories over years to decades under varying stresses. The present work focuses on the latter objective [16].

Recent studies have explored advanced reliability analysis approaches to address complex systems with high-dimensional uncertainties. For example, Bayesian inference-assisted frameworks have been proposed to improve probabilistic modeling accuracy and incorporate multi-source uncertainties in reliability assessment [29]. Similarly, surrogate-based methods leveraging machine learning techniques, such as support vector machines combined with data augmentation strategies, have been introduced to enhance computational efficiency in reliability evaluation [30]. In addition, recent work has explored machine learning-based approaches for predicting the remaining useful life of SiC MOSFETs using data-driven degradation modeling techniques [31].

At the system level, Monte Carlo-based approaches have been widely used for reliability evaluation under stochastic operating conditions, offering improved modeling of uncertainty in converter performance and lifetime prediction [32]. Furthermore, recent review studies have provided comprehensive overviews of reliability modeling techniques for power converters, highlighting the importance of integrating physics-based and system-level modeling approaches [33].

While these approaches significantly improve either modeling accuracy or computational efficiency, many of them focus on system-level reliability estimation without explicitly capturing the coupled electrothermal-aging feedback and progressive device parameter variation under mission profiles. This highlights the need for a unified framework that integrates physics-of-failure-based degradation modeling with mission-profile-dependent electrothermal analysis, as addressed in this work.

1.3 Need for Physics-of-Failure, Electrothermal–Aging, and Mission-Profile Coupling

Long-term reliability evaluation under variable operating conditions is often approached via Monte-Carlo simulation, which samples uncertainty in mission profiles and component behavior to produce lifetime distributions. Previous converter reliability studies have emulated aging using annually updated parameter distributions or time-varying failure-rate models, which can require large numbers of iterations and may still miss the causal feedback between parameter drift, losses, and temperature [3,34].

A physics-of-failure (PoF) approach offers a more transferable alternative for newer technologies: it links stressors to degradation mechanisms using physically motivated models, reducing reliance on extensive historical field data [17]. For SiC MOSFETs, most important aging mechanisms are thermally influenced, implying that aging models must be integrated with electrothermal models that compute junction temperature from losses and ambient conditions [35].

Recent mission-profile-based lifetime prediction methods, e.g., the multi-step condition-mapping strategy in [4], reduce the computational burden by mapping operating conditions to electrothermal stress using precomputed look-up tables and then translating the resulting thermal cycling into lifetime consumption. In addition, mission-profile-based reliability frameworks have been developed for power electronic systems, demonstrating the importance of accurately modeling operating conditions and system-level interactions in reliability evaluation [36,37]. However, such approaches typically treat device parameters as fixed during the mission-profile evaluation and do not explicitly close the loop between aging-induced parameter drift (e.g., R_{dson} increase), the resulting loss/temperature rise, and accelerated further degradation. In contrast, the proposed ET&A framework iteratively updates R_{dson} at short time steps using physics-based chip and package aging models and feeds the updated parameters back into the electrothermal loss/temperature calculation, thereby capturing the reinforcing electrothermal–aging feedback under stochastic mission profiles.

Existing long-term parameter-variation studies have considered package-fatigue-driven resistance rise, while recent evidence indicates that high-temperature-driven chip degradation can dominate R_{dson} drift in power-cycling contexts. Although aging models have been proposed in [35,38] for certain converter classes, a unified PoF-based model for SiC MOSFET three-phase inverters—capable of tracking parameter evolution under stochastic mission profiles in a computationally feasible Monte-Carlo workflow—remains limited [3,35].

1.4 Contributions and Paper Organization

To enable PoF-based Monte-Carlo reliability prediction for SiC MOSFET three-phase inverters under stochastic mission profiles, this paper makes the following contributions:

(1) A comprehensive PoF-based on-state resistance aging model that combines package resistance degradation with chip resistance degradation and translates their combined effects into R_{dson} drift.
(2) A computationally feasible ET&A modeling framework that couples electrical loss estimation, thermal response, and physics-based aging updates to track parameter evolution over long horizons, enabling practical Monte-Carlo reliability prediction under application-specific stochastic mission profiles.

The rest of this paper is organized as follows. Section 2 presents the on-state resistance aging model, including the chip and package submodels and their combination. Section 3 describes the proposed ET&A framework and the simulation flow used to update device parameters under time-varying load and ambient conditions. Section 4 provides numerical validation against published accelerated lifetime test data and demonstrates the approach through an application case study using wind turbine inverter mission profiles. Section 5 concludes the paper and outlines directions for future work.

2 On-State Resistance Aging Model

The aging of R_{dson} can be affected by both chip and package resistance degradation. The experiment results in [38] show that approximately 95% of R_{dson} is due to chip resistance (R_{chip}) and roughly 5% is due to package resistance ($R_{package}$).

$$R_{dson} = R_{chip} + R_{package} \tag{1}$$

This section first presents the aging models for package and chip resistances and later combines them to obtain the comprehensive on-state resistance aging model.

2.1 Package Resistance Aging Model

Package degradation is caused by material fatigue during temperature cycles. The number of cycles to failure at specific stress levels can be estimated by the Coffin-Manson model Eq. (2); the cumulative damage caused by a series of stress cycles can be estimated by the Miner's rule Eq. (3) [16].

$$N_{f_{ji}} = \Delta T_j^{\delta} A \exp\left(\frac{E_a}{k T_{m_i}}\right) \tag{2}$$

$$Q = \sum_{i=1}^{N} \frac{N_i}{N_{f_{ji}}} \tag{3}$$

where ΔT_j is the peak-to-peak value of temperature swing around the mean junction temperature (T_{m_i}), $N_{f_{ji}}$ is the number of cycles to failure at a given ΔT_j and T_{m_i}, E_a is the activation energy, k is the Boltzmann's constant, $Q \in [0,1]$ is the cumulative damage, and N_i is the total number of incident cycles at stress level i.

δ and A are model parameters. The cumulative damage of a SiC MOSFET can be translated to an equivalent increase in package resistance as in Eq. (5) [35].

$$R_{package,0} = R_{dson,0} \cdot w_{package} \tag{4}$$

$$\Delta R_{package} = FL_p \cdot R_{package,0} \cdot Q \tag{5}$$

where $R_{package_{init}}$ is the initial package resistance, $R_{dson,0}$ is the initial on-state resistance (at room temperature), $w_{package}$ (≈5% [38]) is the ratio of the package resistance to total on-state resistance, $\Delta R_{package}$ is the package resistance rise due to fatigue-caused aging, and FL_p is the failure criterion expressed as a percentage of initial package resistance.

2.2 Chip Resistance Aging Model

Chip resistance is composed of several components as shown in Eq. (6) [38].

$$R_{chip} = R_s + R_{ch} + R_A + R_{JEFT} + R_{drift} + R_D + R_{subs} \tag{6}$$

where R_s is the source resistance, R_{ch} is the channel resistance, R_A is the accumulation resistance, R_{JEFT} is the JFET region resistance, R_D is the drain resistance, R_{subs} is the substrate resistance.

Drift resistance is the dominant component in high-voltage SiC MOSFETs [39]. The drift resistance can increase due to the accumulation of electron-hole pair recombination. They depend heavily on the junction temperature. This degradation can be modeled using the Arrhenius model Eq. (7), which describes the device's lifetime under high-temperature stress [40].

$$L\left(T_i\right) = L\left(T_{ALT}\right) \times \exp\left(\frac{E_a}{k}\left(\frac{1}{T_i} - \frac{1}{T_{ALT}}\right)\right) \tag{7}$$

where $L(T_i)$, is the lifetime under an operating temperature T_i estimated based on the lifetime observed under constant temperature stress, T_{ALT}. Here lifetime is defined as the time to reach a prespecified change (e.g., 20%) in chip resistance, as demonstrated in Fig. 2. The total aging caused by a series of temperature stresses $T_{i;i=[1,n]}$ applied for $\Delta t_{i;i=[1,n]}$ periods, respectively, can be given by Eq. (9).

$$R_{chip,0} = R_{dson,0} \cdot w_{chip} \tag{8}$$

$$\Delta R_{chip} = \sum_{i=1}^{n} \frac{FL_c \cdot R_{chip,0}}{L\left(T_i\right)} \Delta t_i \tag{9}$$

where $R_{chip,0}$ is the initial chip resistance, w_{chip} (≈95% [38]) is the ratio of chip resistance to total on-state resistance, ΔR_{chip} is the chip resistance increase, and FL_c is the failure criterion expressed as a percentage of initial chip resistance.

2.3 Effective On-State Resistance Model

The total R_{dson} aging can be described by Eq. (10).

$$\Delta R_{dson} = \Delta R_{package} + \Delta R_{chip} \tag{10}$$

where ΔR_{dson} is the total deviation of R_{dson} due to package and chip resistance deviation. In lifetime prediction and ALTs, the failure criterion is specified as a percentage of the total R_{dson}. In our model, we assume $FL_c = FL_p = FL$, where FL is the failure criterion expressed as a percentage of initial on-state

resistance $R_{dson,0}$ at room temperature. This assumption provides a unified and consistent definition of end-of-life at the system level. Both chip-level and package-level degradation mechanisms ultimately contribute to an increase in the conduction path resistance, which is captured through the variation of R_{dson}. Introducing separate failure criteria would require additional device-specific parameters and coupling rules that are not readily available and would increase model uncertainty. Therefore, a unified failure criterion is adopted as a practical engineering approximation for system-level lifetime prediction.

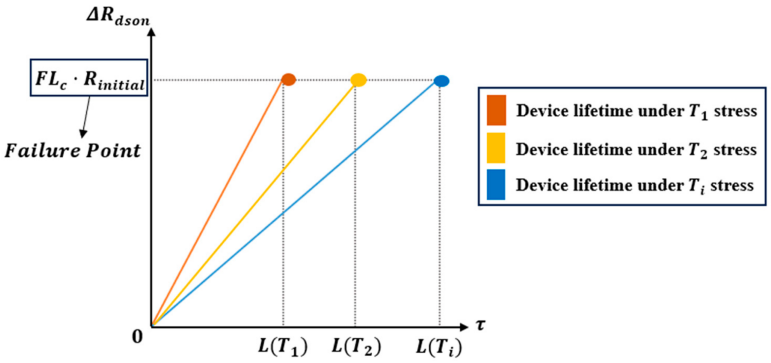

Figure 2: Chip resistance deviation under different temperature stresses.

If the stress is applied for a short time period Δt, the on-state resistance value would increase,

$$R_{dson}\left(t+\Delta t\right) = R_{dson}\left(t\right) + \Delta R_{dson} \tag{11}$$

The effective on-state resistance varies depending on the device temperature as well. The effective on-state resistance R_{dson}^{eff} is given by Eq. (12).

$$R_{dson}^{eff}\left(T_j, t\right) = R_{dson}\left(t\right) \cdot \left[1 + \frac{\alpha}{100}\left(T_j - 25°\mathrm{C}\right)\right] \tag{12}$$

where α is the temperature coefficient, T_j is the junction temperature. The switching and conduction losses are calculated using the effective on-state resistance ($R_{dson}^{eff}\left(t\right)$). The R_{dson} is tracked as a 25°C reference parameter (degradation state). R_{dson}^{eff} is the instantaneous effective value used for loss calculation. The end of life of a device is determined based on the total change of on-state resistance at room temperature (ΔR_{dson}).

3 Proposed Electrothermal and Aging (ET&A) Model

Fig. 3 conceptually illustrates the proposed electrothermal and aging (ET&A) framework. The model iteratively updates the SiC MOSFET parameters under a given mission profile represented by inverter load and ambient temperature variations over a long horizon. The mission profile is discretized at a predefined interval $\Delta\tau$, while the ET&A state update is performed using a smaller simulation step Δt ($\Delta t \leq \Delta\tau$). Within each mission-profile interval, load and ambient conditions are treated as quasi-stationary, and the electrothermal response and aging accumulation are advanced through multiple Δt updates to capture the time-varying degradation dynamics with sufficient numerical resolution.

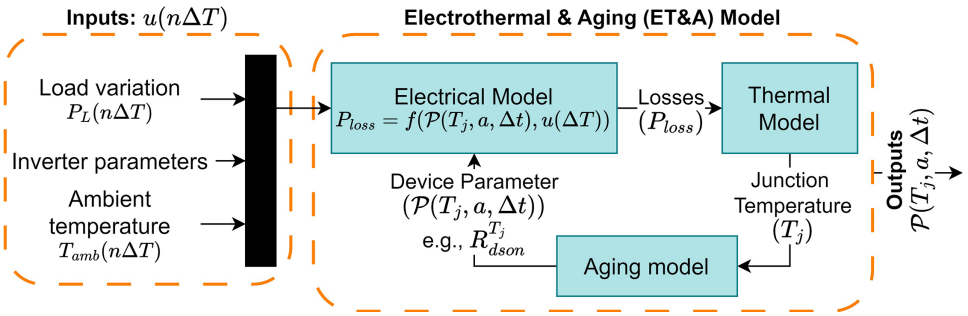

Figure 3: SiC MOSFET electro-thermal & aging (ET&A) model.

At each simulation step, the electrical model computes the average switching and conduction losses corresponding to the instantaneous operating point and the current effective on-state resistance. A simplified Foster-network-based thermal model then estimates the junction temperature using the computed power losses and the ambient temperature. The aging model described in Section 2 updates the degradation state (i.e., the reference on-state resistance) based on the junction-temperature variation over Δt period. To account for temperature-cycling-induced package damage, thermal cycles are extracted from the simulated junction-temperature trace using the half-cycle peak-through counting method adopted in [27], which yields the cycle amplitudes and counts required for Miner's-rule damage accumulation. The updated device parameters are fed back to the electrical and thermal models in the next step, thereby capturing the reinforcing feedback between aging, losses, and junction temperature.

The ET&A model is realized by combining the simplified electrical and thermal models (as referenced in [41]) with the aging model in Section 2, and the overall simulation flow is summarized in Fig. 4. The simulation is initialized at $t = 0$ with $R_{dson} = R_{dson,0}$. For each mission-profile interval, the corresponding load and ambient temperature are applied and the model advances through multiple Δt steps. At each Δt step, power loss and junction temperature are computed, the incremental resistance change ΔR_{dson} is evaluated, and $R_{dson}(t)$ is updated. The simulation terminates when the degradation state reaches the end-of-life criterion (e.g., $R_{dson}(t) \geq (1 + FL)\, R_{dson,0}$), at which point the time-to-failure is recorded.

3.1 Monte-Carlo Simulation

Previous Monte-Carlo simulation methods employed for PE reliability analysis emulated the aging process through annually updated model parameter distributions. This required performing several thousand simulations to reach convergence.

The proposed method uses PoF to predict parameter variations under a given mission profile. A Monte-Carlo simulation described by Algorithm 1 utilizes the steps shown in Fig. 4 to estimate the lifetimes for a sufficiently large set of stochastic mission profiles. Each lifetime simulation is executed in parallel threads.

Algorithm 1: Monte-Carlo simulation

Generate M representative stochastic mission profiles
Do in parallel for each mission profile $m \in [1, M]$
    Perform aging simulation
    S**tore** the lifetime $t(m)$
End do
Read lifetime $t(m)\ \forall m \in [1, M]$
Return [mean lifetime, standard deviation]

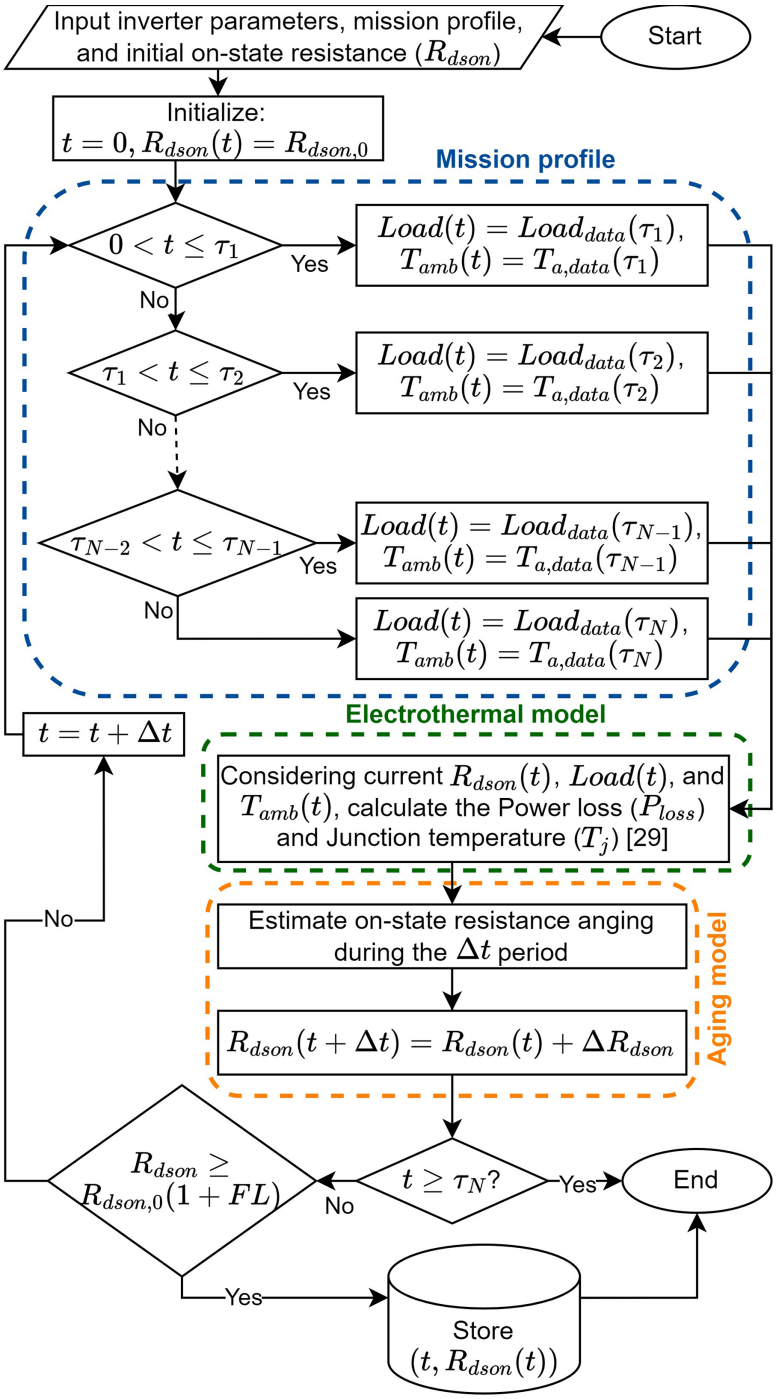

Figure 4: Flowchart of the proposed ET&A model simulation with time-varying load.

3.2 Model Inputs and Calibration

Most of the SiC MOSFET model parameters required for the ET&A simulations are readily found in the product datasheets. The Coffin-Manson model parameters (δ and A) provided in [35] are suitable for a range of SiC MOSFET models. Often activation energy (E_a) is not specified in the datasheets. In our tests, we observe that the aging model can be sensitive to activation energy. The activation energy can vary

depending on the specific design and manufacturing process adopted by different manufacturers. For a given SiC MOSFET sample, using ALT test data we can estimate the activation energy by solving the following parameter fitting problem.

$$\min_{E_a \in R^+} \sum_{n=1}^{N} \left(\hat{R}_{dson}(n) - R_{dson}(n) \right)^2 \tag{13}$$

Subject to,

$$E_{a,min} \le E_a \le E_{a,max} \tag{14}$$

$$\hat{R}_{dson}(n) = f\left(\hat{R}_{dson}(n-1), T_j \right) \tag{15}$$

$$\hat{R}_{dson}(0) = R_{dson,0} \tag{16}$$

where $\hat{R}_{dson}(n)$ and $R_{dson}(n)$ are the simulated and measured on-state resistance in the n^{th} ALT test cycle, $f(\cdot)$ represents the effective on-state resistance model given by Eq. (12). $[E_{a,min}, E_{a,max}]$ represents the typical range of SiC MOSFET activation energy.

4 Numerical Tests and Application Examples

4.1 Comparisons between the R_{dson} Aging Model and the Experimental Data

In this section, the effectiveness of the proposed on-state resistance aging model is compared against the aging experimental data collected from ALT test performed in three different references (on-state resistance and junction temperature variations) [13,14,38]. For each sample, model parameters are summarized in Table 1.

Table 1: SiC MOSFET samples' equivalent model parameters.

Model Parameter	Sample 1 [38]	Sample 2 [13]	Sample 3 [14]
R_{init}	0.06 Ω	0.314 Ω	0.0665 Ω
δ	−5.2776	−5.2776	−5.2776
A	4.9283×10^{13}	4.9283×10^{13}	4.9283×10^{13}
E_a	0.085	0.08	0.213
N_i	0.5	0.5	0.5
B	1.90147×10^{8}	1.90147×10^{8}	1.90147×10^{8}
FL_p, FL_c	20%	20%	20%
α	0.127	0.3	0.2

Sample 1 data is obtained from 60,000 cycles of DC power cycling tests reported in [38]. The sample 2 test data is obtained from [13] where the device under test (DUT) is stressed at 200°C for 60 s and cooled for 120 s; the test is conducted for 500 h. For sample 3, the test data is obtained from [14], where the DUT is stressed at 150°C and cooled at 30°C ambient temperatures for 350 h. The same stress cycles are applied to the simulated SiC model, and the on-state resistance variation due to aging predicted by the proposed model (red) is compared against the actual test data (blue) in Fig. 5. Table 2 compares the final R_{dson} values and overall errors.

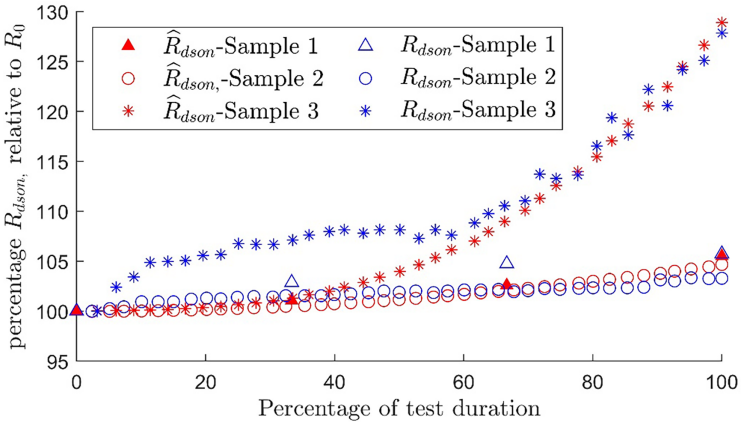

Figure 5: On-state resistance comparison.

Table 2: On-state resistance at the end of ALT tests and that estimated using the proposed model.

	Sample 1 [24]	**Sample 2** [2]	**Sample 3** [4]
Actual	0.07034 Ω	0.32431 Ω	0.085063 Ω
Estimated	0.07019 Ω	0.32876 Ω	0.085766 Ω
Absolute Error	0.00015 Ω (0.213%)	0.00345 Ω (1.05%)	0.000703 Ω (0.86%)

The average percentage error of 1%, 0.45%, and 2.9% are observed for samples 1–3, respectively. The absolute error at the last data point is 0.15, 3.42, and 0.695 mΩ, respectively for samples 1–3 corresponding to 0.213%, 1.05%, and 0.86% percentage error relative to their initial R_{dson} values (R_0).

The results show that the effects of SiC MOSFET aging can be modeled with acceptable accuracy using the proposed model when the model parameters are available. It should be emphasized that the proposed physics-of-failure-based aging model is designed to capture the dominant mechanisms driving long-term degradation, particularly those contributing to progressive increases in on-state resistance. Therefore, the model reproduces the overall aging trend and end-of-life behavior rather than small point-to-point fluctuations in experimental data, which may arise from measurement noise or secondary effects not explicitly modeled. As a result, validation focuses on the accuracy of the final R_{dson} deviation and consistency of the degradation trend.

4.2 ET&A Model Application Example

This section shows how to apply the proposed ET&A model in Monte-Carlo simulations to predict the reliability of a 3-phase inverter of a wind turbine using the mission profile data.

4.2.1 Historical Wind Data Classification

For this example, we utilize one-year wind power output data obtained from a 2 MW wind turbine in a wind farm located in northwestern Taiwan (10-min resolution). We use this dataset to generate a large set of representative daily mission profiles for the next 20 years by following the steps described in Fig. 6.

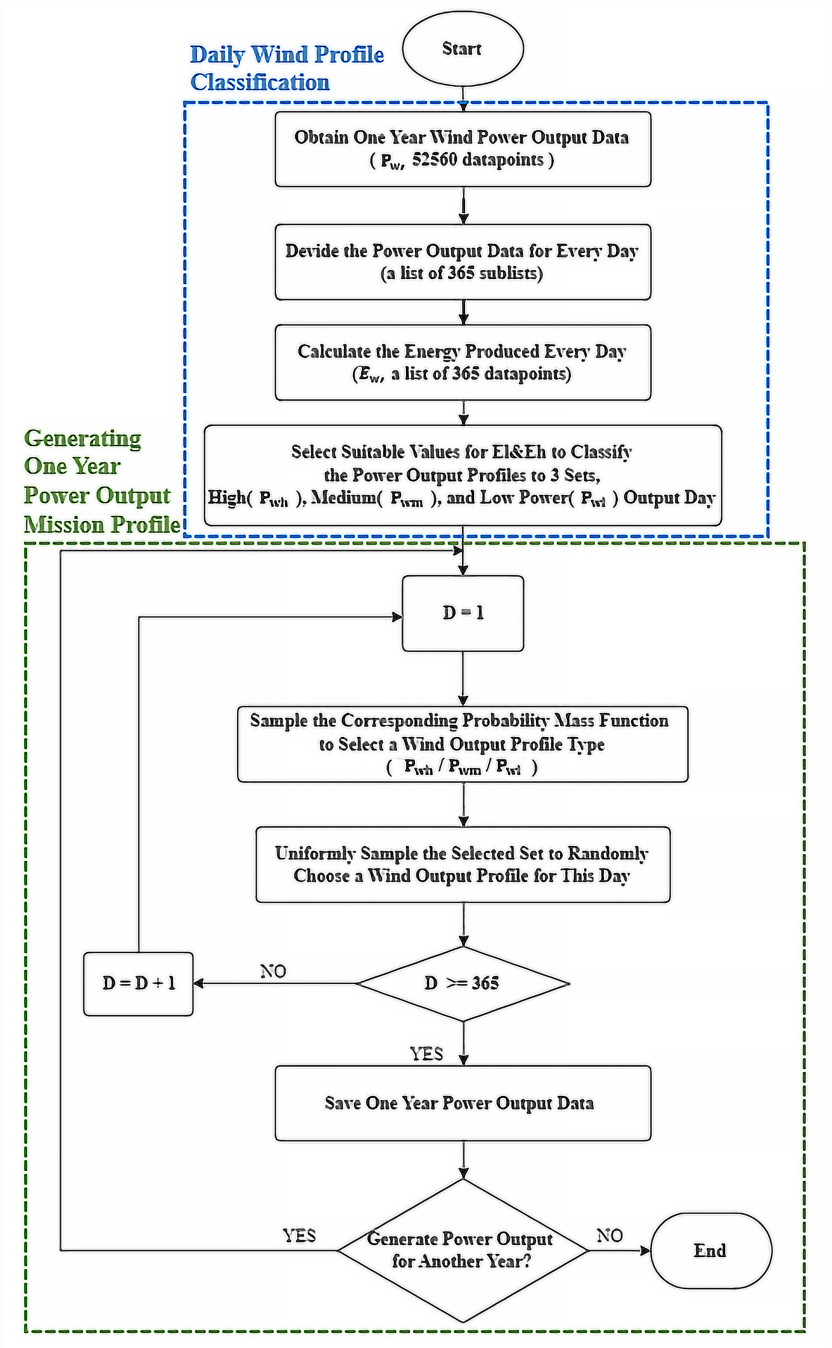

Figure 6: Wind power output profile generation flowchart.

We categorize each day's output as high, medium, or low based on the total energy output. Let $\mathbf{P_w}$ be the set of historical one-year daily wind power output profiles. Define the set $\mathbf{E_w}$ to represent the energy output on each day. ΔT for Eqs. (17) and (18) is 10 min.

$$\mathbf{P_w} = \left\{ \begin{matrix} p^d(t) : d \in [1, 365], \\ t \in [0, 1440]\, \Delta T \end{matrix} \right\} \tag{17}$$

$$\mathbf{E_w} = \begin{Bmatrix} E^d : E^d = \int p^d(t)\, dt, \\ d \in [1, 365], \\ t \in [0, 1440]\, \Delta T \end{Bmatrix} \tag{18}$$

The high ($\mathbf{P_{wh}}$), medium ($\mathbf{P_{wm}}$), and low ($\mathbf{P_{wl}}$) wind output profiles are classified considering the total daily energy output, as shown below.

$$\begin{aligned} \mathbf{P_{wh}} &= \left\{ p^d(t) : p^d(t) \in \mathbf{P_w}, E^d \geq E_h \right\} \\ \mathbf{P_{wm}} &= \left\{ p^d(t) : p^d(t) \in \mathbf{P_w}, E_h > E^d > E_l \right\} \\ \mathbf{P_{wl}} &= \left\{ p^d(t) : p^d(t) \in \mathbf{P_w}, E^d \leq E_l \right\} \end{aligned} \tag{19}$$

where E_h, and E_l are predefined energy thresholds. Fig. 7 shows two sample profiles belonging to each type of wind profile set. Table 3 shows the monthly probability of high, medium, and low power output days as a percentage. From the data set we observe that the wind output is generally high during winter (December–February) and lowest during summer (June–September). Most of the high wind output days occur in winter and spring (March–May).

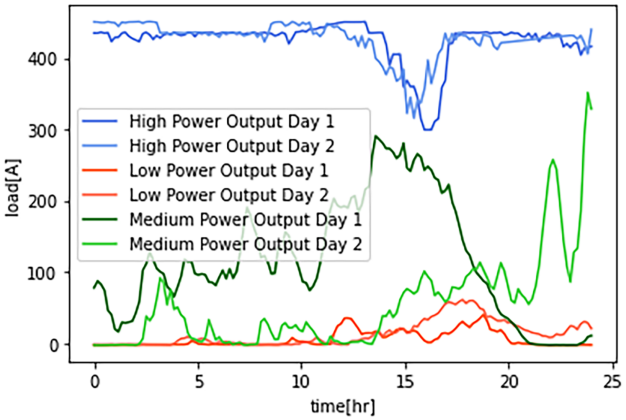

Figure 7: Load data including high, medium, and low load day.

Table 3: Monthly probability of high, medium, and low power output.

Month	$\lvert\mathbf{P_{wh}}\rvert$ (%)	$\lvert\mathbf{P_{wm}}\rvert$ (%)	$\lvert\mathbf{P_{wl}}\rvert$ (%)	Month	$\lvert\mathbf{P_{wh}}\rvert$ (%)	$\lvert\mathbf{P_{wm}}\rvert$ (%)	$\lvert\mathbf{P_{wl}}\rvert$ (%)
Jan.	6.45	83.87	9.6	Jul.	0	63.33	36.66
Feb.	20	70	10	Aug.	0	60	40
Mar.	13.33	56.66	30	Sep.	0	56.66	43.33
Apr.	3.33	83.33	13.33	Oct.	0	90	10
May	0	70	30	Nov.	0	86.66	13.33
Jun.	0	80	20	Dec.	2.94	94.11	2.94

4.2.2 Generation of Representative Random Mission Profiles

For Monte-Carlo simulations, the mission profiles representing the next 20 years could be generated considering long-term climate variations and monthly wind energy generation probabilities. For brevity, this example uses the fixed seasonal high, medium, and low wind energy output probabilities, shown in Table 4, for the whole study period. When climate change-induced wind pattern variations are forecasted for a specific site, the seasonal wind speed probabilities can be specified for each year to reflect the forecasted variations.

Table 4: Probability of output power characteristics in different seasons considered for the Monte-Carlo simulations.

	Winter	Spring	Summer	Fall
High	60%	40%	10%	60%
Medium	30%	40%	40%	30%
Low	10%	20%	50%	10%

To generate the daily wind output profiles using the specified generation probabilities, we take the following steps: (1) sample the corresponding seasonal wind energy output probability mass function (Table 4) to pick one of three sets $\mathbf{P_{hw}}$, $\mathbf{P_{mw}}$, $\mathbf{P_{lw}}$; (2) from the selected set, uniformly sample one daily profile. (Using a similar method, one can generate ambient temperature profiles based on the one-year temperature data. For this example, we use the one-year temperature data obtained from the Taiwan Central Weather Bureau). For this Monte-Carlo simulation, we generate 1000 randomized 20-year mission profiles.

4.2.3 Inverter Configuration and Device Parameters

We assume a wind turbine with a three-phase inverter based on high-power SiC MOSFET produced by Wolfspeed (model: CAB650M17HM3) [42]. This SiC MOSFET is rated for 1.7 kV and 650 A. Four inverters are connected in parallel to support the peak 2 MW output power. For brevity, we assume the four inverters are identical. Thus, each inverter handles one-fourth of the power generated by wind turbines.

Most of the SiC MOSFET parameters needed for the ET&A model can be obtained from the datasheet. If the manufacturer does not provide the activation energy, it can be estimated using ALT data and solving the parameter fitting problem as demonstrated in Section 3.2. The SiC MOSFET model parameters considered in this simulation are shown in Table 5.

Table 5: Model parameters considered for the wind turbine inverter.

Parameter	Value	Parameter	Value
1st Miller Plateau Voltage	9.5 V	Max. Output Capacitance	2 nF
2nd Miller Plateau Voltage	10.5 V	Min. Output Capacitance	0.06 nF
Gate Resistance	10 Ω	Inverter Dc-link Voltage	1.2 kV
Threshold Voltage	2.5 V	Voltage Modulation Index	0.85
Gate Driver Voltage	15/−4 V	δ	−5.2776
Input Capacitance	100 nF	A	4.9×10^{13}
On State Resistance	1.42 mΩ	E_a	0.2
Switching Frequency	30 kHz	k	8.62×10^{-5}eV/K
FL	0.2	N_i	0.5
α	0.3	B	1.9×10^{8}

The partition of 95% chip resistance and 5% package resistance is adopted from literature as a representative approximation. In practice, this ratio may vary depending on device design, packaging technology, and manufacturing variations, and can be experimentally characterized through dedicated measurements, such as those reported in [28]. In the absence of device-specific data for the considered module, this approximation is used to enable the modeling framework. It is noted that different partitions may influence the quantitative lifetime estimates; however, a detailed sensitivity analysis is beyond the scope of this study and can be considered in future work.

4.2.4 ET&A Simulation

Following the steps described in Fig. 4, we run the 20-year ET&A simulation and repeat it for each of the 1000 mission profiles generated. The time to failure is computed by observing the time taken for the on-state resistance to change by 20% (alternative failure percentage can be adopted by the user based on the application-specific requirements). The lifetime observed in all 1000 simulations is approximated by a normal distribution, as shown in Fig. 8. In this example, the mean lifetime is 11.683 years (with a standard deviation of 0.074 years). These results depend on the SiC MOSFET parameters and the wind output variations considered in this study. For reference, we estimated the lifetime of the inverter when its output remains constant at a value equivalent to the average power output of the wind turbine. In this case, the lifetime increases to 16.7 years due to reduced temperature cycles and lower peak junction temperatures. Considering only the average inverter loading and neglecting the power output variations can overestimate the lifetime by ~34%. This highlights the significance of PoF-based Monte-Carlo approach for long-term reliability studies in SiC MOSFET devices; it captures the fatigue-related package degradation and high temperature-related chip degradation accurately. Additional simulations with increased sample sizes were conducted to verify convergence of the lifetime distribution. The results showed negligible variation in the mean and standard deviation beyond 1000 samples, confirming that the chosen sample size is sufficient.

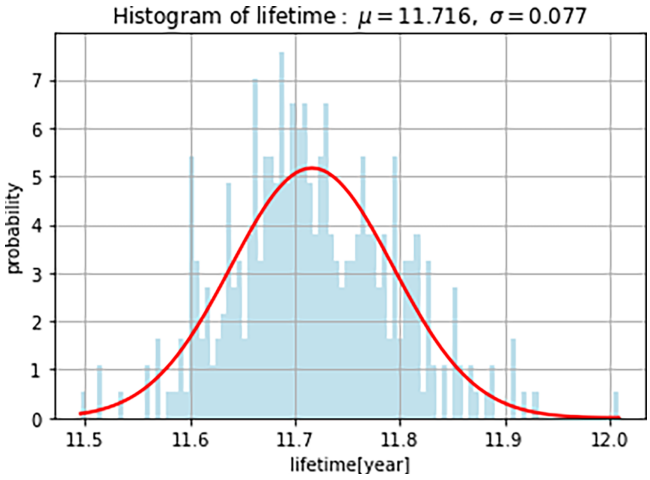

Figure 8: Lifetime histogram and approximate normal distribution obtained using the Monte-Carlo simulations.

Although these simulations were performed using the available limited information on SiC MOSFET model parameters and mission profiles, the results demonstrate the feasibility of conducting a detailed Monte-Carlo simulations considering SiC aging dynamics.

This simulation was performed using Python 3.12 on a computer equipped with an Intel i9-12900 processor and 32 GB RAM. The computational time for performing the 20-year simulations 1000 times is about 11.5 h (equivalent to ~40 s for executing one 20 years simulation).

5 Conclusions and Future Directions

This paper presents a unified PoF-based ET&A framework for predicting the long-term reliability of SiC MOSFET-based three-phase inverters operating under stochastic mission profiles. By integrating electrical loss modeling, thermal response, and coupled chip–package aging mechanisms, the proposed approach enables dynamic tracking of on-state resistance degradation and its feedback effect on device stress.

The effectiveness of the proposed aging model is validated against multiple ALT datasets, demonstrating strong agreement with experimental results. The model achieves low relative errors in predicting the final on-state resistance deviation, confirming its capability to capture the end-of-life behavior of SiC MOSFETs under different stress conditions.

The application study using real wind turbine mission profile data highlights the practical importance of the proposed framework. Monte Carlo simulations based on stochastic operating conditions predict a mean inverter lifetime of approximately 11.68 years, with a standard deviation of 0.074 years. In contrast, reliability estimation based solely on average load conditions leads to a lifetime prediction of approximately 16.7 years, resulting in an overestimation of about 34%. This clearly demonstrates that neglecting mission-profile variability can lead to significantly optimistic lifetime predictions.

Overall, the proposed ET&A framework provides a computationally feasible and physically grounded approach for reliability assessment of SiC MOSFET-based power converters, enabling more accurate lifetime prediction in applications with highly variable operating conditions.

While the proposed framework demonstrates promising results, several limitations should be acknowledged. The model relies on certain simplifying assumptions, such as the use of a single degradation indicator (on-state resistance) and approximate partitioning between chip and package resistance contributions due to limited device-specific data. In addition, some model parameters, such as activation energy, require calibration based on accelerated test data, which may vary across devices and manufacturers.

Future work will focus on extending the proposed framework to incorporate multiple degradation indicators and more detailed device-level modeling, including the interaction of electrical, thermal, and mechanical failure mechanisms. Furthermore, the integration of device-specific characterization, condition monitoring data, and high-fidelity mission profile forecasting could further improve prediction accuracy. The application of the proposed methodology to other converter topologies and real field reliability datasets will also be explored.

To objectively compare the traditional approach against the proposed reliability analysis method, sufficient reliability field data from SiC MOSFET 3-phase inverters must be collected. Furthermore, the feasibility of incorporating the proposed method in the inverter design process for a specific applications can be explored.

Acknowledgement: The authors highly appreciate the support from the Industrial Technology Research Institute (ITRI) for providing their valuable insights for this research. We also thank Prof. Chan-nan Lu for providing the wind farm data.

Funding Statement: This research was funded by ITRI and The APC was funded by National Science and Technology Council grant 114-2222-E-110-006.

Author Contributions: The authors confirm contribution to the paper as follows: Conceptualization, Mohammed Ansar Mohammed Manaz and Tzung-Lin Lee; methodology, Mohammed Ansar Mohammed Manaz and Shang Ping Hong; software, Mohammed Ansar Mohammed Manaz, Shang Ping Hong and Tzung-Lin Lee; validation, Mohammed Ansar Mohammed Manaz and Shang Ping Hong; formal analysis, Mohammed Ansar Mohammed Manaz and Shang Ping Hong; investigation, Mohammed Ansar Mohammed Manaz and Shang Ping Hong; resources, Mohammed Ansar Mohammed Manaz and Tzung-Lin Lee; data curation, Mohammed Ansar Mohammed Manaz and Shang Ping Hong; writing—original draft preparation, Shang Ping Hong; writing—review and editing, Mohammed Ansar Mohammed Manaz, Shang Ping Hong and Tzung-Lin Lee; visualization, Mohammed Ansar Mohammed Manaz and Shang Ping Hong; supervision, Mohammed Ansar Mohammed Manaz and Tzung-Lin Lee; project administration, Mohammed Ansar Mohammed Manaz and Tzung-Lin Lee; funding acquisition, Mohammed Ansar Mohammed Manaz and Tzung-Lin Lee. All authors reviewed and approved the final version of the manuscript.

Availability of Data and Materials: Data not available due to legal restrictions. The data underlying this study were provided by a third-party source under a confidentiality agreement. As such, the raw data cannot be shared publicly.

Ethics Approval: This study does not include any human or animal subjects.

Conflicts of Interest: The authors declare no conflicts of interest.

Nomenclature

Acronyms and Abbreviations

AC-PC	Alternating-current power cycling
ALT	Accelerated life test
CMB	Chopper-mode bias
CTE	Coefficient of thermal expansion
DC-PC	Direct-current power cycling
DUT	Device under test
ET&A	Electrothermal and aging (framework/model)
FEA/FEM	Finite-element analysis/finite-element method
GaN	Gallium nitride
HTGB	High-temperature gate bias
HTGS	High-temperature gate switching
IGBT	Insulated-gate bipolar transistor
MC	Monte Carlo
MOSFET	Metal–oxide–semiconductor field-effect transistor
PE	Power electronics/power electronic
PoF	Physics of failure
Si	Silicon
SiC	Silicon carbide
TC	Thermal cycling
TSEP	Temperature-sensitive electrical parameter
WBG	Wide bandgap

Symbols and Variables

Electrical/Device Parameters

R_{dson}	On-state drain–source resistance at reference temperature unless noted [Ω]
$R_{dson,0}$	Initial on-state resistance at room temperature (reference) [Ω]
R_{chip}	Chip resistance component of R_{dson} [Ω]
$R_{package}$	Package resistance component of R_{dson} [Ω]
ΔR_{dson}	Total change in R_{dson} due to aging (evaluated at room temperature) [Ω]

ΔR_{chip}	Change in chip resistance due to aging [Ω]
$\Delta R_{package}$	Change in package resistance due to aging [Ω]
w_{chip}	Fraction of R_{dson} attributed to chip resistance
$w_{package}$	Fraction of R_{dson} attributed to package resistance
$R_{dson}(t)$	Aged on-state resistance at time t (reference temperature) [Ω]
$R_{dson}^{eff}(T_j, t)$	Effective on-state resistance accounting for junction temperature [Ω]
α	Temperature coefficient of on-state resistance [%/°C]
V_{th}	Gate threshold voltage [V]
V_{bd}	Body-diode forward voltage (TSEP) [V]
$R_{g,int}$	Internal gate resistance [Ω]
$I_{g,lk}$	Gate leakage current [A]
$I_{ds,lk}$	Drain–source leakage current [A]

Thermal/Stress Variables

T_j	Junction temperature [K]
T_{amb}	Ambient temperature [K]
ΔT_j	Junction temperature swing (peak-to-peak) [K]
$T_{m,i}$	Mean junction temperature for stress bin i [K]
Z_{th}	Thermal impedance (e.g., Foster-network equivalent) [K/W]

Aging/Lifetime Model Parameters

$N_{f,ji}$	Number of cycles to failure at stress level i
N_i	Number of cycles accumulated at stress level i
Q	Miner's cumulative damage index ($0 \le Q \le 1$)
A, δ	Coffin–Manson model coefficients
E_a	Activation energy [eV]
k	Boltzmann constant used in this work ($k = 8.617 \times 10^{-5}$ eV/K) [eV/K]
F_L	End-of-life criterion as allowable fractional increase in R_{dson} (e.g., 0.2)
$F_{L,p}$	Package-level failure criterion
$F_{L,c}$	Chip-level failure criterion
$L(T_i)$	Lifetime at operating temperature T_i (Arrhenius-based scaling) [time]
T_{ALT}	ALT reference temperature used in Arrhenius scaling [K]
τ_i	Duration of stress interval i [time]

Time Discretization/Simulation Variables

Δt	Aging simulation time step (parameter update step) [s]
$\Delta \tau$	Mission-profile discretization interval [s]
τ_N	Total simulated mission duration
t_f	Time to failure (when R_{dson} reaches the failure criterion)
M	Number of Monte Carlo mission profiles

Mission Profile Variables (Wind Energy Case Study)

$p_d(t)$	Wind power output profile for day d [W]
P_w	Set of daily wind power output profiles over the historical year
E_d	Total energy output for day d [Wh]
E_w	Set of daily energy outputs over the historical year
E_h, E_l	Energy thresholds for classifying days as high/medium/low [Wh]
P_{wh}, P_{wm}, P_{wl}	Sets of high/medium/low daily profiles

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